Sub-threshold Modeling of Short-Channel Effects (SCEs) in Double-Gate (DG) MOSFETs

A Thesis Submitted

in Partial Fulfillment of the requirement

for the degree of

Master of Technology

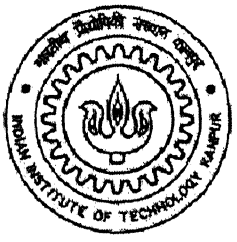
By

Gaurav Chhabra

Under the Supervision

of

Dr. S. Qureshi



to the

Department of Electrical Engineering

Indian Institute of Technology Kanpur

2005

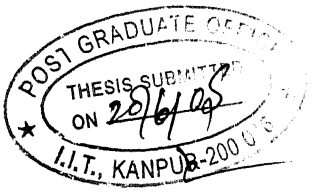
CERTIFICATE

This is to certify that the work contained in the thesis titled "**Sub-threshold Modeling of Short Channel Effects (SCEs) in Double Gate (DG) MOSFETs**" by Gaurav Chhabra (Roll. No. Y3104029) has been done under my supervision and that this work has not been submitted elsewhere for the award of a degree or diploma.

21/6/05

June 2005

Thesis Supervisor
Dr. S. Qureshi
Professor
Electrical Engineering Department
Indian Institute of Technology
Kanpur-208016
India



Acknowledgements

I wish to express my sincere gratitude to my supervisor Prof. S. Qureshi for his invaluable guidance and advice during every stage of this endeavour. I am grateful to him for his continuing encouragement and support without which, it would not have been possible for me to complete this work successfully. His insightful comments and suggestions have continually helped me to improve my understanding.

I am also thankful to the faculty of electrical engineering department for teaching us the various courses especially Dr. Aloke Dutta who taught us 'Device Modeling' which is the foundation course for my thesis work. I am also thankful to all those who have been associated with VLSI lab for providing me the necessary infrastructure in completing my work.

I would like to thank my friends Bodhraj, Chander Pal, Talari Manojaya, Sudhir Bapna, Ravi Kumar M. N., Sandeep Garg, Dipanjan Basu, Saurabh Sharma and all those whose name I am not able to put here but have given me emotional strength to go on and finish this work successfully.

In the end I would like to thank my parents for being a constant support during my whole course work.

Gaurav Chhabra

Dedicated to

My Niece (Amishi)

Abstract

Double-Gate (DG) MOSFETs are becoming the most promising device structures for scaling in nanometer range. In view of anticipated role of DG MOSFET in digital, analog and mixed signal device applications, modeling and simulation of the device behaviour has assumed considerable importance. In this work Sub-threshold behavior, which determines the switching characteristics and the short-channel immunity of the device, has been studied. Physics based analytical sub-threshold model for un-doped DG MOSFET is proposed. The model results were compared with numerical simulation results of 2-D device simulator (ATLAS). A good agreement was found between the proposed model and the numerical simulation results. The strength of the model is that it is physics based and simple and yet capable of predicting the device behaviour reasonably accurately.

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Abbreviations and Symbols

1. MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
2. SOI	Silicon On Insulator
3. VLSI	Very Large Scale Integration
4. DG	Double Gate
5. GAA	Gate All Around
6. DIBL	Drain Induced Barrier Lowering
7. ε_{si}	Permittivity of silicon (F cm^{-1})
8. t_{si}	Silicon body thickness (nm)
9. φ	Electric Potential (V)
10. ε_{ox}	Permittivity of oxide (F cm^{-1})
11. E_{ox}	Field in oxide (Vcm^{-1})
12. Q_i	Mobile charge carrier density (C cm^{-2})
13. t_{ox}	Oxide thickness (nm)
14. φ_s	Surface Potential (V)
15. φ_{centre}	Potential at centre of silicon film (V)
16. V_G	Gate Voltage (V)
17. $V_{FB,f}$	Front-Gate Flat-Band Voltage (V)
18. $V_{FB,b}$	Back-Gate Flat-Band Voltage (V)
19. k	Boltzman's Constant (1.38 x 10^{-23} J K^{-1})
20. T	Temperature (300 K)
21. q	Charge on electron (1.6e-19 C)

22. n_i	Intrinsic carrier density (cm^{-3})
23. C_{ox}	Oxide Capacitance per unit area (Fcm^{-2})
24. η	Fitting parameter
25. V_{FB}	Flat-Band Voltage (V)
26. λ	Characteristic Length (nm)
27. ϕ_{bi}	Built-In Voltage (V)
28. V_{DS}	Drain to Source Voltage (V)
29. E_G	Band-Gap of Silicon (1.12 eV)
30. V_{Geff}	Effective Gate Voltage (V)
31. L	Channel Length (nm)
32. SCIBL	Short-Channel Induced Barrie Lowering
33. J_n	Electron Current Density ($A\ cm^{-2}$)
34. J_p	Hole Current Density ($A\ cm^{-2}$)
35. $J_{n,drift}$	Electron Drift Current density ($A\ cm^{-2}$)
36. $J_{p,drift}$	Hole Drift Current Density ($A\ cm^{-2}$)
37. $J_{n,diff}$	Electron Diffusion Current Density ($A\ cm^{-2}$)
38. $J_{p,diff}$	Hole Diffusion Current Density ($A\ cm^{-2}$)
39. D_n	Diffusion Constant ($cm^2 sec^{-1}$)
40. I_{DS}	Drain Current (A)
41. $V_{channel}$	Channel Voltage (V)
42. ϕ_t	Thermal Voltage (V)
43. μ_n	Mobility of Electrons ($cm^2\ V^{-1}\ sec^{-1}$)
44. $y_{\min}$	Minimum Potential Point (nm)
45. $\varphi_{s\min}$	Minimum Surface Potential (V)
46. S	Sub-threshold Swing (mV/decade)

47. $E_{ox,f}$	Front-Gate Oxide Field (Vcm^{-1})
48. $E_{ox,b}$	Back-Gate Oxide Field (Vcm^{-1})
49. $\varphi_{s,f}$	Front-Gate Surface Potential (V)
50. $\varphi_{s,b}$	Back-Gate Surface Potential (V)
51. C_{si}	Silicon Body Capacitance per unit area (Fcm^{-2})
52. α	Gate Coupling Factor
53. $V_{Geff,f}$	Front-Gate Effective Voltage (V)
54. $V_{Geff,b}$	Back-Gate Effective Voltage (V)
55. $y_{\min,b}$	Back Surface Minimum Potential Point (nm)
56. V_t	Threshold Voltage (V)
57. E_F	Fermi Level
58. E_i	Intrinsic Fermi Level

Chapter 1

Introduction

1.1 Overview

Bulk-MOSFET and SOI-MOSFET have been in the area of VLSI for past many years. Devices have been scaling down, as the process technologies are improving, for faster speeds. But as one is scaling down into the nanometer range the gate tunneling currents and short-channel effects are coming into picture, which affect the proper functioning of the devices. This has lead to increased research towards coming up with newer devices with improved performance without adding to processing complexity. One of the intuitive methods of controlling the short-channel effects as one goes down in length is to somehow increase the gate control over the channel length. For this, multi-gate MOSFETs like double-gate (DG) MOSFETs, Π-gate or Fin-FET, and gate all around (GAA) MOSFET [1],[2],[3],[4] are being studied. Of these newer structures, double-gate (DG) MOSFET is becoming major area of research, as it has shown the ability to scale down to very small lengths with acceptable short-channel effects without adding significantly to processing complexity. It has been anticipated that it will not only be used in digital domain but will also be extensively used in analog and mixed signal applications.

All around the world effort is being put to come up with a compact model for DG MOSFETs so that its characteristics can be analyzed by simulation and also to determine the maximum scaling limits to which it can be scaled down. Many models have been proposed till now. Some are based on the modeling of inversion charge [5],[6]. In the paper by Jin He et. al [5], they have started with one dimensional Poisson's equation and instead of solving it for potential, they have solved it for inversion charge and then used that expression of inversion charge to evaluate potential and current in the device. But models based on inversion charge have an inherent disadvantage that the moderate inversion regime of device operation is not that effectively modeled, as is modeled by surface potential based model. For DG MOSFETs several surface potential based models have been proposed [7], [8], [9].

One such model was proposed by Yuan Taur [9] in which he has came up with a model for drain current of DG MOSFETs with undoped body. But this model has a problem that it is not analytical model and needs to be solved iteratively. In another model by Malobabic et. al [10], they have simplified the model for drain current to come up with an analytical model. But all these models deal with long channel devices. Thus a model is needed for short channel devices.

Since these devices have shown good immunity to short-channel effects and due to their anticipated use in analog and mixed signal applications, sub-threshold region becomes an important area to be given special attention. Till now many works have been published on DG MOSFET. But as far as sub-threshold region specifically is concerned, only one model for sub-threshold is proposed by X. Liang et. al [11] . In this work they have solved the 2-D Laplace's equation in terms of series solutions and then they came up with an expression for the characteristic length for scaling of devices and also an expression for potential variation in two dimensions. The model is able to predict the device behaviour in sub-threshold region quiet accurately along with the threshold voltage roll-off, drain induced barrier lowering (DIBL) effect and sub-threshold slope. But the inherent problem with the model is that it is not analytically solvable and even after making simplifying assumptions numerical iterations can not be avoided. In the present work, attempt is made to come up with an analytical model for sub-threshold region with reasonable accuracy and much simpler formulation, ultimately resulting in faster calculations.

In earlier works on sub-micrometer MOSFETs by Zhi-Hong Liu et. al [12], a model for surface potential in sub-threshold region has been formulated based on the application of Gauss's law to the silicon body. They have taken the effect of lateral field also while applying Gauss's law. Since the formulation was done for sub-threshold region, the inversion charge was considered negligible compared to ionized dopants and was neglected. They have also given the expression for characteristic length for scaling with only one fitting parameter in the model. The model has shown to predict the results reasonably accurately for lengths down to 100 nm.

A model based on similar formulation obtained by application of Gauss's law to the fully depleted SOI MOSFETs has been proposed by Srinivasa R. Banna et. al [13] . In this model they have applied Gauss's law to the box of SOI MOSFET, again

taking into account the flux due to lateral field and neglecting the mobile charge carriers compared to ionized dopants. Similar expressions for simple bulk-MOSFETs were obtained. Again the model was able to predict the surface potential variation in the device very accurately.

As already mentioned, in the case of DG MOSFETs only one model for sub-threshold region has been reported. The inherent difficulty in DG MOSFETs is the variation of potential in the direction perpendicular to channel, i.e. from one gate to another gate. Thus this results in need for non-analytical solution for the potential at the center of the silicon body film. This renders the solution to be solved by using numerical / iterative methods. This is true for Liang and Taur [11] model which is solvable only by numerical iterations. Thus there is a need for making simplifying assumptions to come up with an analytical model for potential variation.

The basic device structure that is used for the formulation of models is as shown below.

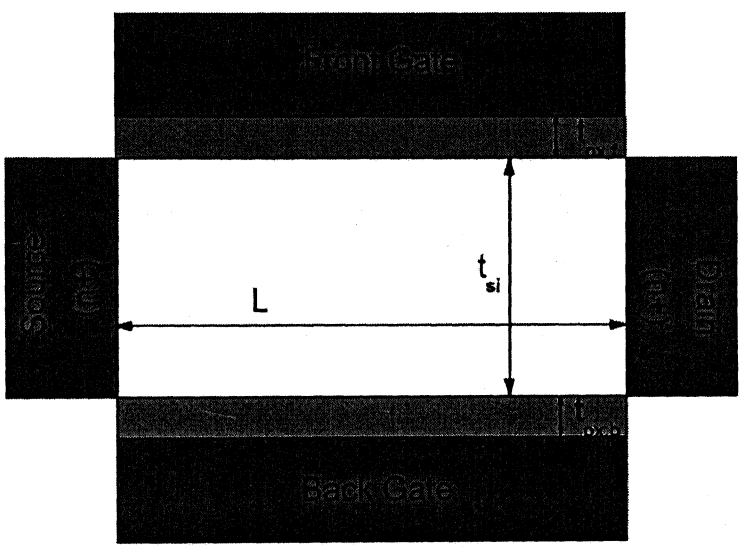

Figure 1.1. Basic Device Structure

DG MOSFET can operate in two modes: Symmetric and Asymmetric Mode. In symmetric mode, the line of symmetry of device goes through the center of the silicon body or one can say that everything is same for front gate and back gate namely,

oxide thickness, oxide material and gate work –function. Same gate voltage is applied to both the front and the back gate. The device can be operated in asymmetric model by driving front and back gate independently or by having different oxide thickness or by having different gate work functions or by having combination of any of these methods. Thus from the above discussion it becomes clear that to come up with a model for such a device, both modes need to be considered separately.

1.2 Organization of thesis

This work has been divided into two parts based on operation mode discussed above. Part I will look into the formulation of the model for symmetric DG MOSFET with chaper 2 dealing with formulation of surface potential expression along the channel and chapter 3 dealing with the formulation of the sub-threshold current model, sub-threshold slope formulation and the comparisons of the results obtained using model with 2-D device simulator ATLAS [14].

Part II consists of chapter 4 and 5 with chapter 4 dealing with the formulation of surface potential expressions and chapter 5 dealing with formulation of current expression in sub-threshold region for asymmetric DG MOSFET in similar way as done for symmetric case.

In the end in chapter 6 a comparison is done between symmetric and asymmetric mode and the models for symmetric and asymmetric modes are combined to give a generalized model for DG MOSFETs in sub-threshold region.

Chapter 2

Modeling of Surface-Potential along the channel in the Sub-Threshold Region using Gauss's Law

2.1 Gauss's Law

Gauss Law is one of the most widely used laws in electrostatics. It is not only used in semiconductor devices but is used anywhere there is an electric flux and accumulation of charge. For geometries of sufficient symmetry, it simplifies the calculation of the electric field. In mathematical form it can be represented as,

$$\oint \vec{E} . d\vec{A} = \frac{Q}{\varepsilon_r \varepsilon_0}$$

where $\vec{E}$ is the electric field $d\vec{A}$ is the normal to the surface and Q is the net charge contained within the surface.

In the case of semiconductors there can be two kind of charges - one due to the ionized dopants and other due to mobile charge carriers i.e. electrons and holes. Gauss's Law will be applied within the silicon body of the DG MOSFET, which for present case is undoped. The device structure that will be considered for analysis is shown in Figure 2.1. Applying the Gauss's Law to the silicon body of the DG MOSFET

$$-\varepsilon_{si} \int_{-t_{si}/2}^{t_{si}/2} \frac{\partial \varphi(x,y)}{\partial y}\, dx - 2\,\varepsilon_{ox} \int_{0}^{y} E_{ox}(y')\, dy' = Q_i\, t_{si}\, y \qquad (2.1)$$

where the first term on the L.H.S represents the net electric flux entering the silicon body from the lateral direction and the second term represents the net electric flux entering the body from the top and bottom. The R.H.S represents the net charge within the body.

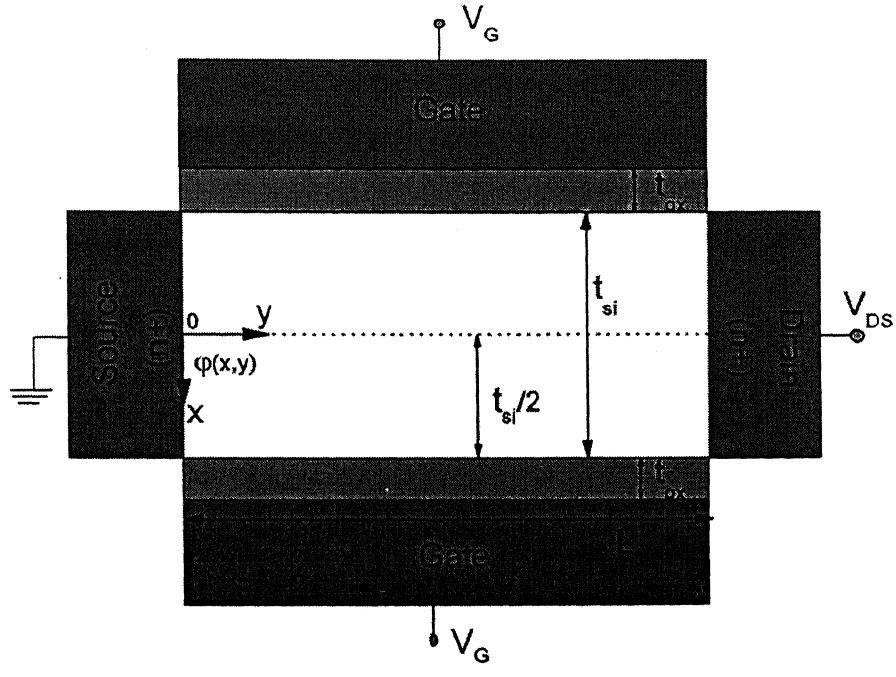

Figure 2.1. Symmetric Double-Gate (DG) MOSFET structure

Sub-threshold region will be considered for the present case. Hence the mobile charge carriers will be neglected. Thus Eq. (2.1) becomes

$$-\varepsilon_{si}\int_{-t_{si}/2}^{t_{si}/2}\frac{\partial\varphi(x,y)}{\partial y}\,dx-2\,\varepsilon_{ox}\int_{0}^{y}E_{ox}(y')\,dy'=0 \qquad (2.2)$$

2.2 Assumption for flux entering from lateral direction

In Eq. (2.2), as mentioned earlier, the first term on L.H.S represents the net electric flux entering the silicon body from the lateral direction i.e. source and drain side. It has been shown in the earlier works of Suzuki et. al [15] and supported by Yuan Taur [16] that in the sub-threshold region, the difference between the surface potential φ_s and the potential at the centre of the silicon body φ_{centre} is very small or in other words it can be said that the variation of potential in the x-direction (or perpendicular) direction is negligible. To support this argument figure 2.2 and figure 2.3 show the variation of surface potential and centre potential with respect to gate voltage, V_G.

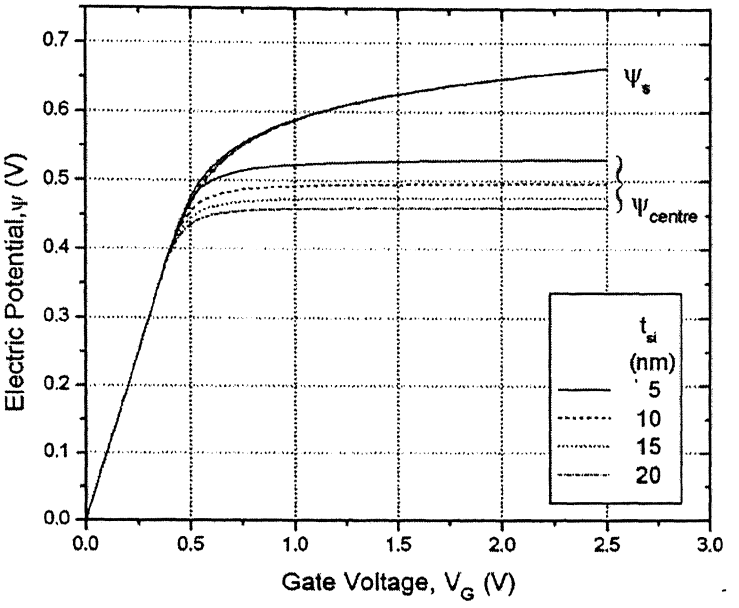

Figure 2.2. Surface potential and centre potential comparison with silicon body thickness, t_{si} varying from 5nm to 20nm in steps of 5nm, oxide thickness, t_{ox} = 1.5nm and $V_{FB,f} = V_{FB,b} = 0.0$ V

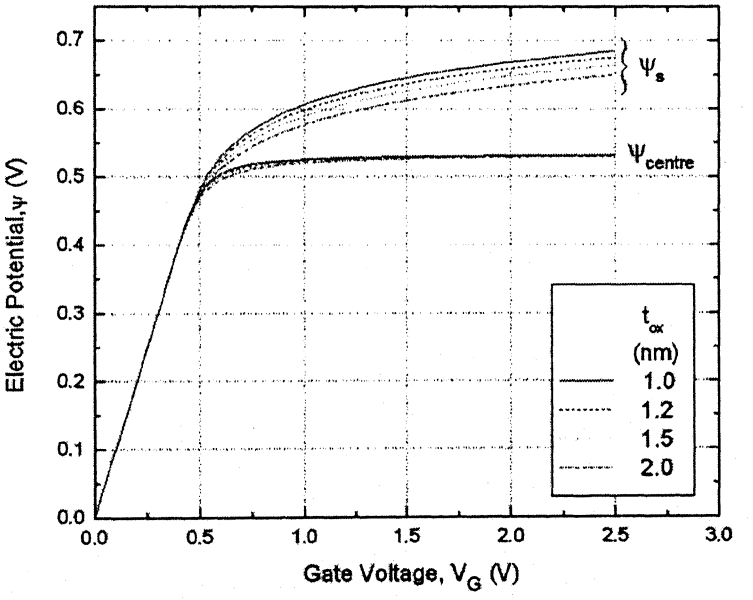

Figure 2.3. Surface potential and centre potential comparison with oxide thickness, t_{ox} varying as 1.0nm, 1.2nm, 1.5nm and 2.0nm, silicon body thickness, t_{si} = 5nm and $V_{FB,f} = V_{FB,b} = 0.0$ V

Figure 2.2 and figure 2.3 are obtained by solving numerically the following equation

$$V_G - V_{FB} = \varphi_{centre} - \frac{2kT}{q}\ln\left[\cos(\theta)\right] - \frac{\sqrt{2\varepsilon_{si}kTn_i}}{C_{ox}}\exp\left(\frac{q\varphi_{centre}}{2kT}\right)\tan(\theta) \tag{2.3}$$

where $\theta = \sqrt{\frac{q^2 n_i}{2\varepsilon_{si}kT}}\exp\left(\frac{q\varphi_{centre}}{2kT}\right)\frac{t_{si}}{2}$

The derivation of Eq. (2.3) is given in Appendix A. Here the surface potential in terms of centre potential is given as

$$\varphi_s = \varphi_{centre} - \frac{2kT}{q}\ln\left[\cos(\theta)\right] \tag{2.4}$$

Thus from figure 2.2 and figure 2.3 it is clear that in the sub-threshold region the surface potential and the centre potential are almost the same. The results have been verified by 2-D device simulator [14]. Hence $\varphi(x, y)$ can assumed constant in the x-direction. Based on this the following assumption is made

$$\int_{-t_{si}/2}^{t_{si}/2} \frac{\partial\varphi(x,y)}{\partial y}\,dx = \frac{t_{si}}{\eta}\frac{d\varphi_s(y)}{dy} \tag{2.5}$$

where η[†] is the fitting parameter [12], [13] which depends upon the oxide thickness, silicon body thickness and channel length. For short channel devices potential is not constant along the perpendicular direction due to strong effect of lateral fields. Still the difference between the surface potential and centre potential is not significant and hence the parameter η has been introduced. Thus from Eq. (2.5) it is clear that the 2-dimensional (2-D) problem effectively reduces to a 1-dimensional (1-D) problem.
Eq. (2.2) and Eq. (2.5) give

$$\frac{\varepsilon_{si}t_{si}}{\eta}\frac{d\varphi_s(y)}{dy} + 2\varepsilon_{ox}\int_0^y E_{ox}(y')\,dy' = 0 \tag{2.6}$$

Now $E_{ox}(y')$ is the field coming from the gates and is given by

$$E_{ox}(y) = \frac{\left[V_G - V_{FB} - \varphi_s(y)\right]}{t_{ox}} \tag{2.7}$$

[†] Refer section 3.5.1

Putting Eq. (2.7) into Eq. (2.6) and differentiating with respect to y

$$\frac{\varepsilon_{si} t_{si}}{\eta} \frac{d^2 \varphi_s(y)}{dy^2} + \frac{2\varepsilon_{ox}}{t_{ox}} \left[V_G - V_{FB} - \varphi_s(y) \right] = 0$$

or

$$\frac{d^2 \varphi_s(y)}{dy^2} = \frac{1}{\lambda^2} \left[\varphi_s(y) - (V_G - V_{FB}) \right] \tag{2.8}$$

where $\lambda = \sqrt{\frac{\varepsilon_{si} t_{si} t_{ox}}{2\eta \varepsilon_{ox}}} \equiv Characteristic\ Length$

2.3 Formulation of boundary Conditions

Now to formulate the boundary conditions an undoped body DG MOSFET is assumed with n+ source and drain and since the silicon body is undoped, free charge carriers are assumed to be negligible.

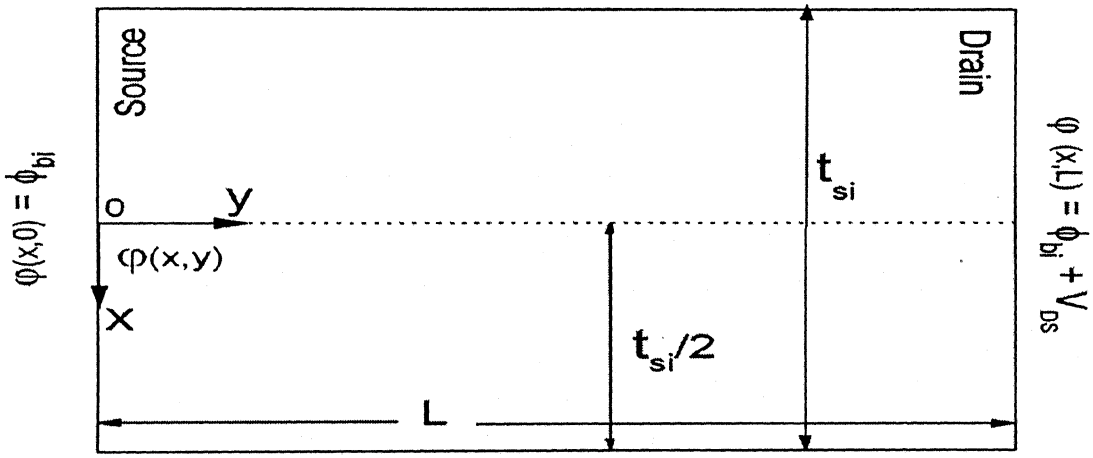

Figure 2.4. Boundary conditions for Short-Channel Symmetric DG MOSFET based on Gauss law.

The boundary conditions, as shown in figure 2.4, are

$$\varphi_s(0) = \varphi(x,0) = \phi_{bi} \tag{I}$$

$$\varphi_s(L) = \varphi(x,L) = \phi_{bi} + V_{DS} \tag{II}$$

Now (I) comes from the fact that source/drain is heavily doped and body is undoped, hence treated as a step-graded junction. The body being undoped results in a potential drop in the body, known as the built-in potential ϕ_{bi} and can be expressed as, [11]

$\phi_{bi} = \frac{E_G}{2q}$ = Work-function difference between n^+ source/drain and intrinsic body.

(II) is same as (I) only the drain junction is reversed biased by an additional bias of V_{DS} and body being undoped, this potential also drops across the body resulting in boundary condition (II).

2.4 Analytical Model for Surface Potential in Sub-threshold Region

Eq. (2.8) is a standard differential equation and can be solved easily along with the boundary conditions (I) and (II)‡ to give the following expression for the surface potential along the channel in the sub-threshold region

$$\varphi_s(y) = V_{Geff} + \left(\varphi_s(0) - V_{Geff}\right)\left(\frac{\sinh\left(\frac{L-y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}\right) + \left(\varphi_s(L) - V_{Geff}\right)\left(\frac{\sinh\left(\frac{y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}\right) \qquad (2.9)$$

where $V_{Geff} = V_G - V_{FB}$

From Eq. (2.9) it is evident that for short-channel devices, surface potential is not constant as is also verified in [12], [13]. Figure 2.5 and figure 2.6 show the calculated results based upon Eq. (2.9) along with its comparison with the 2-D numerical simulations obtained using Atlas device simulator.

From figure 2.5 and figure 2.6 it is clear that as the channel length is decreased, potential no longer remains constant along the channel. Although the potential is not constant near the source/drain region but that is due to the source-body and drain-body junction and not due to the short-channel effects. In figure 2.7 and figure 2.8, the variation of surface potential along the channel for larger values of drain voltage is shown, showing the validity of the model for higher V_{DS}.

‡ *Refer Appendix B*

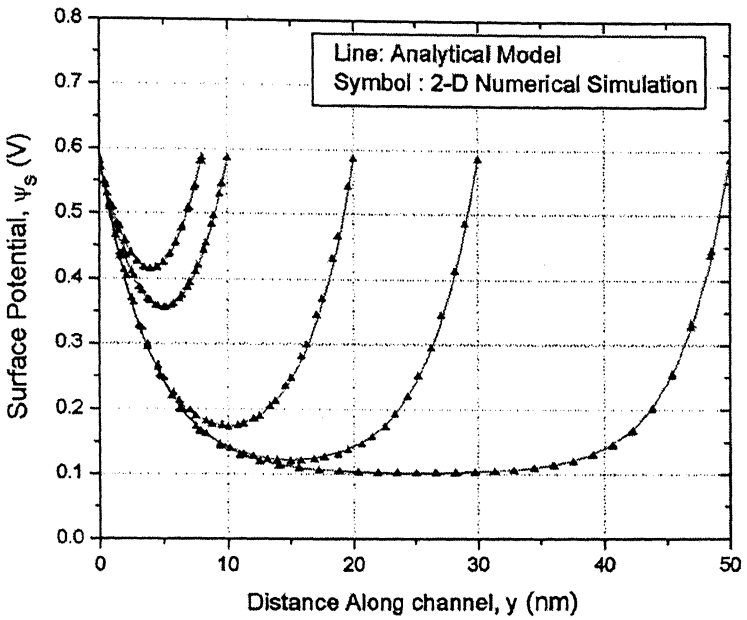

Figure 2.5. Comparison of Surface Potential along channel for analytical model Eq. (2.9) and 2-D Numerical Simulation (short lengths) for small drain bias (V_{DS} = 0.01 V), t_{ox} = 1.5 nm, t_{si} = 5nm, V_G = 0.1 V, $V_{FB,f} = V_{FB,b}$ = 0.0 V, L=8, 10, 20, 30 and 50 nm.

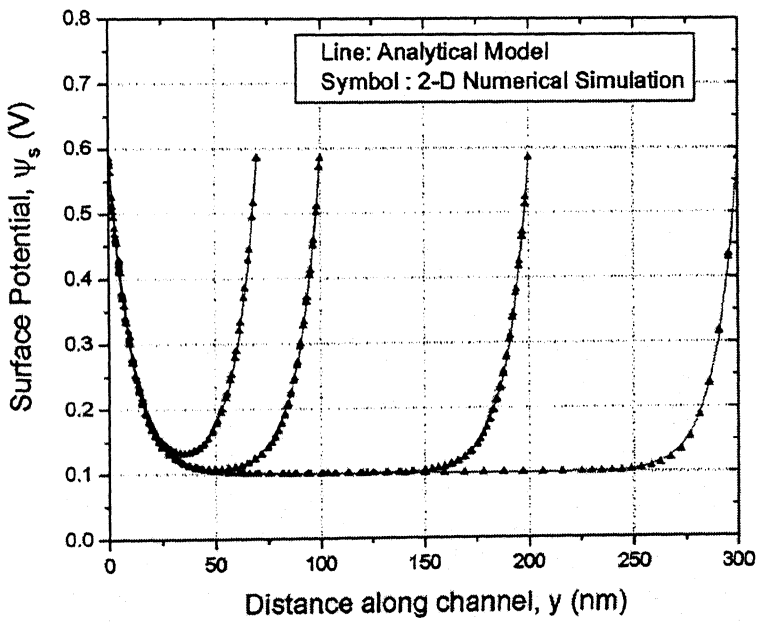

Figure 2.6. Comparison of Surface Potential along channel for analytical model Eq. (2.9) and 2-D Numerical Simulation (longer lengths) for small drain bias (V_{DS} = 0.01 V), t_{ox} = 1.5 nm, t_{si} = 5nm, V_G = 0.1 V, $V_{FB,f} = V_{FB,b}$ = 0.0 V, L=70, 100, 200 and 300 nm.

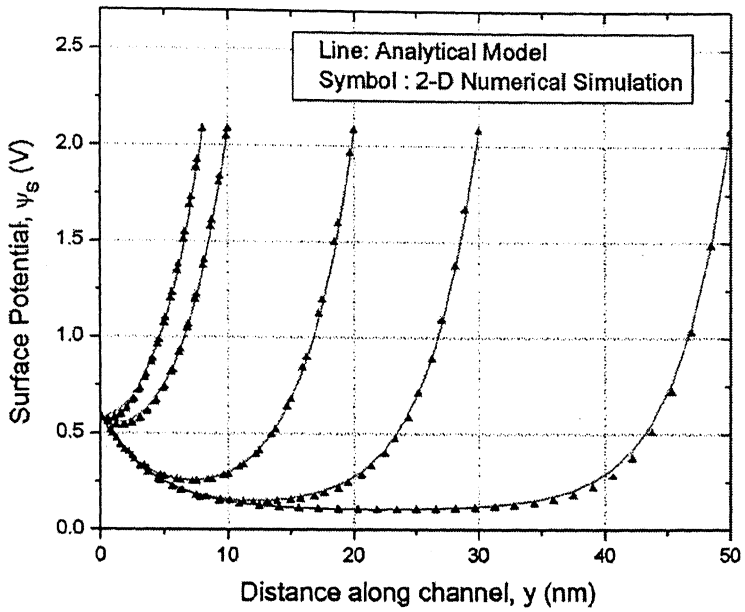

Figure 2.7. Comparison of Surface Potential along channel for analytical model Eq. (2.9) and 2-D Numerical Simulation (short lengths) for large drain bias (V_{DS} = 1.5 V), t_{ox} = 1.5 nm, t_{si} = 5nm, V_G = 0.1 V, $V_{FB,f} = V_{FB,b}$ = 0.0 V, L=8, 10, 20, 30 and 50 nm.

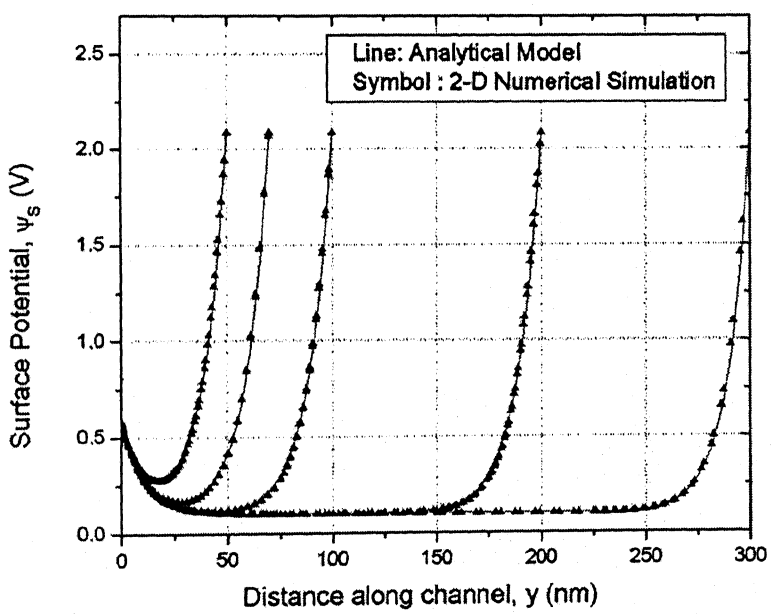

Figure 2.8. Comparison of Surface Potential along channel for analytical model Eq. (2.9) and 2-D Numerical Simulation (longer lengths) for large drain bias (V_{DS} = 1.5 V), t_{ox} = 1.5 nm, t_{si} = 5nm, V_G = 0.1 V, $V_{FB,f} = V_{FB,b}$ = 0.0 V, L=70, 100, 200 and 300 nm.

In figure 2.9 and figure 2.10 both plots of surface potential for low and high values of V_{DS} are compared and it clearly shows that for long channel devices even for higher drain biases, the minimum potential along the channel remains unaffected while for shorter length devices, the surface potential is raised clearly portraying the effect of lateral field. This increase in minimum potential along the channel due to increase in lateral field is effectively reducing the barrier to mobile charge carriers to flow from source to drain and hence results in reduction in the threshold voltage of the device. This effect of reduction of threshold voltage with increase in drain voltage is known as Drain Induced Barrier Lowering (DIBL). Even at lower drain biases, the minimum potential along the channel keeps on increasing as the length is decreased as was shown earlier in figure 2.5. This is due to reduction in channel length. Thus is known as Short-Channel Induced Barrier Lowering (SCIBL) [18]. This effect of reduction in threshold voltage with decrease in channel length has been attributed to increase in the charge shared by the source-channel and drain-channel depletion regions. This effectively reduces the amount of charge required by gate to form the channel and hence the threshold voltage.

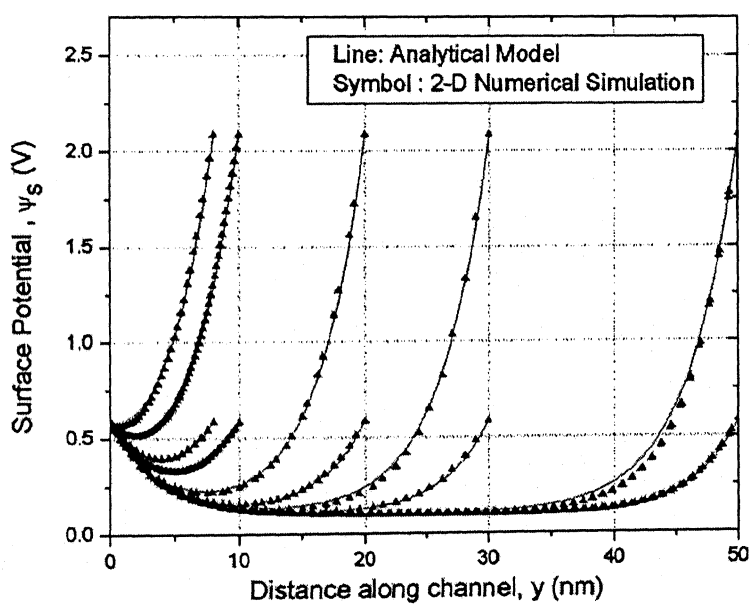

Figure 2.9. Effect of drain induced barrier lowering (DIBL) for short lengths and comparison with 2-D Numerical Simulation t_{ox} = 1.2 nm, t_{si} = 5nm, V_G = 0.1 V, $V_{FB,f} = V_{FB,b}$ = 0.0 V, L=8, 10, 20, 30 and 50 nm and V_{DS} = 0.01 and 1.5 V

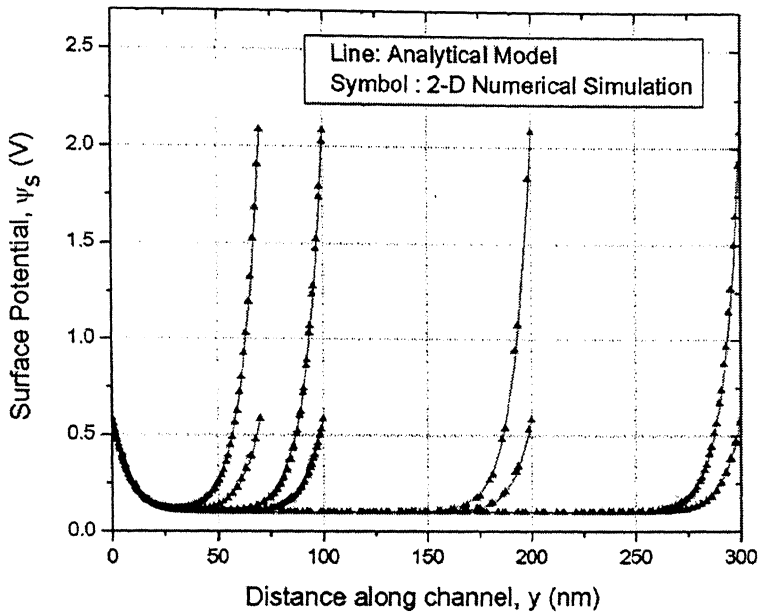

Figure 2.10. Effect of drain induced barrier lowering (DIBL) for short lengths and comparison with 2-D Numerical Simulation t_{ox} = 1.2 nm, t_{si} = 5nm, V_G = 0.1 V, $V_{FB,f} = V_{FB,b}$ = 0.0 V, L=70, 100, 200 and 300 nm and V_{DS} = 0.01 and 1.5 V

2.5 Effect of Oxide Thickness on surface potential

Using Eq. (2.9) surface potential is plotted along the channel and compared with the 2-D numerical simulation showing the variation in surface potential due to the variation in oxide thickness. Figure 2.11 gives a clear picture that keeping everything else constant and reducing the oxide thickness results in reduction of minimum value of the surface potential along the channel showing that more gate voltage will be required to form the channel for thinner oxides and thus predicting increased threshold voltage with decrease in the oxide thickness. This effect is more pronounced in the shorter length devices compared to long channel devices. Similar things were observed by Wong et. al [19].

2.6 Effect of Silicon Body Thickness on surface potential

Looking at figure 2.12 it can be found that as the silicon body thickness is decreased the minimum potential along the channel keeps on decreasing and thus showing increased coupling between the two channels formed in the device. This results in increased volume inversion in the silicon body. Thus more gate voltage is

required to form the channel under the gates, resulting in increase in threshold voltage with decrease in the silicon body thickness.

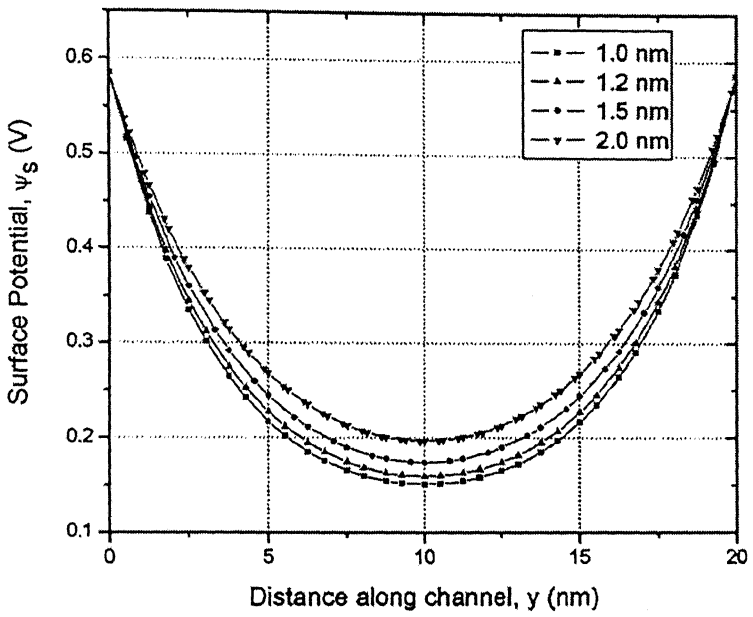

Figure 2.11. Effect of oxide thickness variation on surface potential along channel. L=20 nm, t_{si}=5 nm, V_G = 0.1 V, V_{DS} = 0.01V, $V_{FB,f} = V_{FB,b}$ = 0.0 V

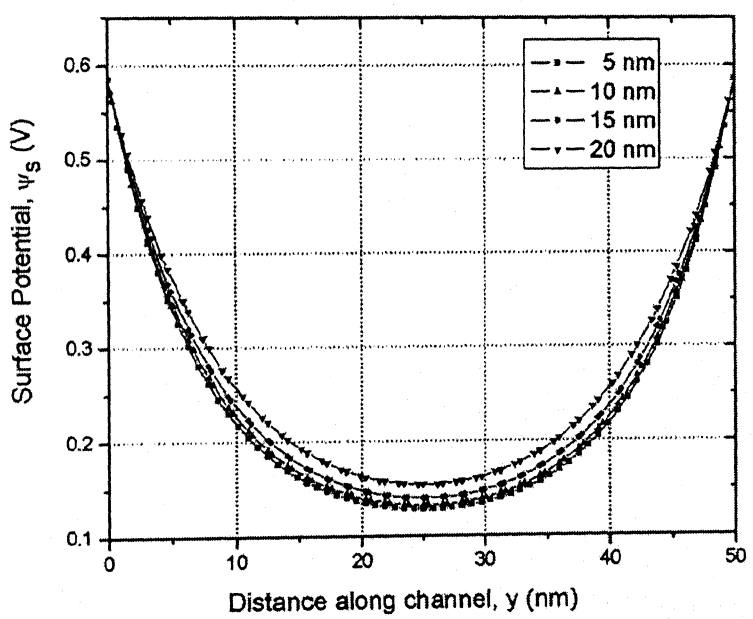

Figure 2.12. Effect of silicon body thickness variation on surface potential along channel. L=50nm, t_{ox}=2 nm, V_G = 0.1 V, V_{DS} = 0.01V, $V_{FB,f} = V_{FB,b}$ = 0.0 V

Chapter 3

Modeling of Sub-Threshold Current

In this chapter first an analytical model for sub-threshold current for a long channel DG MSOFET will be derived and then it is shown how it can be converted to a model for short-channel devices using the expression for the surface potential derived in chapter 2.

Ideally it is expected that when the gate voltage is below the threshold voltage there should be no current but in reality the situation is different. Even when gate voltage is below the threshold voltage there are some charge carriers, which are very small but not exactly zero. So this leads to the flow of some finite drain current even when gate voltage is less than threshold voltage. This is what is know as the sub-threshold leakage and this constitutes the sub-threshold current.

It has already been shown with the help of simulation and also on the basis of physics based models that diffusion of carriers is the main mechanism of charge transport in the sub-threshold region. In sub-threshold region some of the minority carriers are able to overcome the barrier at source-channel region and are then swept to the drain due to the lateral field and this constitutes the sub-threshold current.

3.1 Diffusion current

In a semiconductor at any time the current density at any instant is given by

$$J_n = J_{n,drift} + J_{n,diff} \tag{3.1}$$

$$J_p = J_{p,drift} + J_{p,diff} \tag{3.2}$$

Thus both drift current and diffusion current make up the total current in a semiconductor. They may not be occurring at the same time, but the equation is still valid. In the sub-threshold region the dominant mechanism is diffusion current as mentioned earlier. For a long-channel device it has been assumed that the potential along the channel is constant which results in a zero electric field thus making contribution due to drift current, to sub-threshold current, zero. But as the channel length is reduced this assumption of constant surface potential along the channel is no longer valid and thus the minimum potential along the channel needs to be found out

which will be used for calculating the diffusion current, as at the point of minimum potential the electric field will be zero. This results in the total current due to diffusion current. Also for a short channel device the point of minimum potential is unique unlike long-channel devices where there is a large part along the length where potential is constant. Thus in sub-threshold region re-writing the equations for current densities

$$J_n = J_{n,diff} \tag{3.3}$$

$$J_p = J_{p,diff} \tag{3.4}$$

As an n-DG MOSFET will be considered so the current due to electrons will be calculated. Similar formulations can be obtained for a p-DG MOSFET by replacing n with p and q with –q. Diffusion current can be expressed as

$$J_{n,diff} = qD_n \frac{dn}{dy} \tag{3.5}$$

where D_n = diffusion constant and,

$\frac{dn}{dy}$ = concentration gradient of minority carriers

3.2 Long Channel Current Formulation

From Eq. (3.5) the expression for sub-threshold current is given as [17]

$$I_{DS} = qD_n W t_{si} \frac{dn}{dy} \tag{3.6}$$

In present case there is volume inversion, as reported in [20], hence the complete silicon body thickness is taken. Thus the current flows through whole of the silicon body.

If $V_{channel}(y)$ is the potential variation along channel direction due to applied drain bias, then the expression for the carrier concentration variation with distance from source is given as

$$n(y) = n_i \exp\left(\frac{\varphi_s(y) - V_{channel}(y)}{\phi_t}\right) \tag{3.7}$$

Now for a long-channel device the surface potential along the channel is assumed to be constant with value

$$\varphi_s = V_G - V_{FB} \tag{3.8}$$

Thus this results in modification of Eq. (3.7) to

$$n(y) = n_i \exp\left(\frac{V_G - V_{FB} - V_{channel}(y)}{\phi_t}\right) \tag{3.9}$$

where $\phi_t = \frac{kT}{q} \equiv Thermal\ Voltage$

Thus using Eq. (3.9) in Eq. (3.6) and integrating from source to drain

$$I_{DS} = qD_n \frac{W}{L} t_{si}\left[n_i \exp\left(\frac{V_G - V_{FB}}{\phi_t}\right) - n_i \exp\left(\frac{V_G - V_{FB} - V_{DS}}{\phi_t}\right)\right]$$

or

$$I_{DS} = qn_i t_{si} D_n \frac{W}{L} \exp\left(\frac{V_G - V_{FB}}{\phi_t}\right)\left[1 - \exp\left(\frac{-V_{DS}}{\phi_t}\right)\right] \tag{3.10}$$

Also Einstein's relation relates diffusion coefficient to the mobility as follows

$$D_n = \phi_t \mu_n \tag{3.11}$$

Thus expression for a long channel device, sub-threshold current is

$$I_{DS} = qn_i t_{si} \mu_n \phi_t \frac{W}{L} \exp\left(\frac{V_G - V_{FB}}{\phi_t}\right)\left[1 - \exp\left(\frac{-V_{DS}}{\phi_t}\right)\right] \tag{3.12}$$

3.3 Short Channel Current Formulation

Eq. (3.12) will work fine for the devices where surface potential is constant for a large part of channel length. But as the length is decreased further, the potential does not remain constant along the channel, which is the underlying assumption made in the derivation of Eq. (3.12). Since potential is not constant so minimum potential along the channel is found at the point where electric field will be zero. This will result in zero contribution due to drift current. For evaluating minimum surface potential, Eq. (2.9) is differentiated and equated to zero to give the point along the channel where the surface potential will be minimum. The minimum potential point along the channel (y_{min}) is given by

$$y_{\min} = \frac{\lambda}{2}\log\left[\frac{(\varphi_s(0) - V_{Geff})\exp\left(\frac{L}{\lambda}\right) - (\varphi_s(L) - V_{Geff})}{(\varphi_s(L) - V_{Geff}) - (\varphi_s(0) - V_{Geff})\exp\left(\frac{-L}{\lambda}\right)}\right] \tag{3.13}$$

Now using this value of $y_{\min}$ and evaluating surface potential at this point using Eq. (2.9), the value of minimum surface potential along the channel is given by

$$\varphi_{s\min} = V_{Geff} + \frac{1}{C_1}\sqrt{2C_2(\varphi_s(0) - V_{Geff})(\varphi_s(L) - V_{Geff}) - V_{DS}^2} \tag{3.14}$$

where

$$C_1 = \sinh\left(\frac{L}{\lambda}\right) \qquad \text{and}$$

$$C_2 = \cosh\left(\frac{L}{\lambda}\right) - 1$$

It can be seen by calculations that for a long-channel device where (L >> λ) Eq. (3.14) reduces to Eq. (3.8) thus resulting in a unification of surface potential for long channel and short channel device. The derivation for Eq. (3.13) and Eq. (3.14) is given in Appendix C.

Diffusion current is evaluated at minimum potential point along channel, as is done by Liang et.al [11], as sub-threshold conduction is determined by the minimum potential along the channel which would produce the maximum barrier to carrier flow. Thus to get expression for short-channel sub-threshold current the value of surface potential of long channel is replaced with the minimum surface potential expression as given in Eq. (3.14). Now looking at Eq. (3.12), the surface potential for a long-channel is given by $(V_G - V_{FB})$ term. Thus replacing this with $\varphi_{s\min}$ the following expression for sub-threshold current for a short-channel device is obtained

$$I_{DS} = qn_i t_{si}\mu_n \phi_t \frac{W}{L}\exp\left(\frac{\varphi_{s\min}}{\phi_t}\right)\left[1 - \exp\left(\frac{-V_{DS}}{\phi_t}\right)\right] \tag{3.15}$$

3.3 Sub-threshold Swing Formulation

One of the important performance measurement parameter for a MOSFET in sub-threshold region is amount of gate voltage swing required to switch device from its ON state to OFF state. This gate voltage swing is called inverse Sub-threshold slope (S). It is defined as the amount of change in gate voltage required for producing

one-decade change in sub-threshold current. So for achieving better switching characteristics it should be small as possible. Clearly, S is a convenient measure for turn-off characteristics of a MOSFET. By definition it is given as [17]

$$S = \left[\frac{d(\log I_{DS})}{dV_G}\right]^{-1} = 2.303\left[\frac{d(\ln I_{DS})}{dV_G}\right]^{-1} \qquad (mV/decade) \tag{3.16}$$

Now from Eq. (3.15)

$$\frac{d(\ln I_{DS})}{dV_G} = \frac{1}{\phi_t}\frac{d\varphi_{s\min}}{dV_G} = \frac{1}{\phi_t}\frac{d\varphi_{s\min}}{dV_{Geff}} \tag{3.17}$$

Using Eq. (3.14) one gets

$$\frac{d\varphi_{s\min}}{dV_{Geff}} = 1 + \frac{2C_2\left|\varphi_s(0) - V_{Geff} + \varphi_s(L) - V_{Geff}\right|}{2C_1\sqrt{2C_2\left(\varphi_s(0) - V_{Geff}\right)\left(\varphi_s(L) - V_{Geff}\right) - V_{DS}^2}}$$

$$= 1 + \frac{C_2\left|\varphi_s(0) + \varphi_s(L) - 2V_{Geff}\right|}{C_1\sqrt{2C_2\left(\varphi_s(0) - V_{Geff}\right)\left(\varphi_s(L) - V_{Geff}\right) - V_{DS}^2}} \tag{3.18}$$

Thus final sub-threshold swing expression for symmetric DG MOSFET is given as

$$S = 2.303\,\phi_t\left[1 + \frac{C_2\left[\varphi_s(0) + \varphi_s(L) - 2V_{Geff}\right]}{C_1\sqrt{2C_2\left(\varphi_s(0) - V_{Geff}\right)\left(\varphi_s(L) - V_{Geff}\right) - V_{DS}^2}}\right]^{-1} \tag{3.19}$$

In Eq. (3.19) it can be seen that the sub-threshold swing is dependent upon V_G through V_{Geff}. So to make sure that device is well within sub-threshold region and for comparison with the results obtained with 2-dimensional device simulation V_G is kept as $10\,\phi_t$

3.5 Results of comparison with 2-D numerical simulation

The basic device structure shown in chapter 2 is made in 2-D device simulator and simulated using Atlas, which solves the basic device equations like Poisson's equation, continuity equation at the grid points created in simulator by discretizing these equations and solving iteratively for various bias points at each of the grid point. Mid-gap gates† are considered in both numerical simulation and analytical model calculations. Results have been verified by varying channel length from 300 nm down

† *Refer Appendix A*

to 10 nm, silicon thickness from 5 nm to 20 nm in steps of 5 nm and 4 oxide thickness values of 1.0 nm, 1.2 nm, 1.5 nm and 2.0 nm are used. Along with that constant mobility model is used with mobility value of 1400 $cm^2V^{-1}sec^{-1}$.

3.5.1 Current Comparison Results

Figures 3.1 – 3.4 show the comparison of model results with numerical simulations for different oxide thickness and silicon body thickness with a maximum error of 20% in case of short-channel devices. The normalized sub-threshold current (I_{DS} x L/W) obtained using analytical model (Eq. 3.15) is compared with 2-D numerical simulator [12] results for various lengths, silicon body thickness and oxide thickness and parameter η values are obtained. Using these values of η and exponential regression analysis the following expression for η is obtained with coefficient of determination (COD) value of 0.95.

$$\eta = e^{(1.364)} t_{si}^{(0.2617)} t_{ox}^{(0.67358)} L^{(-0.88869)} \tag{3.20}$$

where L, t_{si}, t_{ox} are in nm.

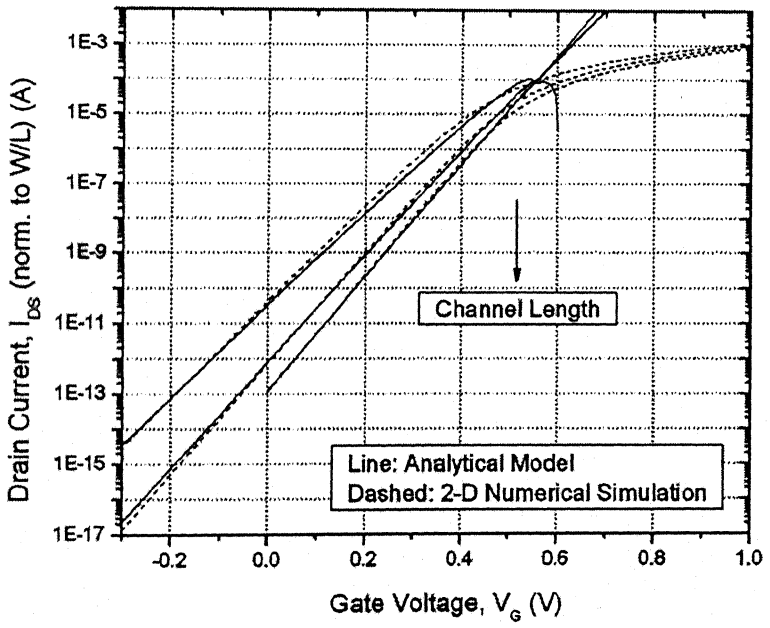

Figure 3.1. Comparison of analytical current model Eq. (3.15) with 2-D atlas simulation for varying lengths. V_{DS}=1.0 V, t_{si} = 5 nm, t_{ox} = 1.5 nm, L = 20, 30 and 50 nm, $V_{FB,f} = V_{FB,b}$ = 0 V, mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$

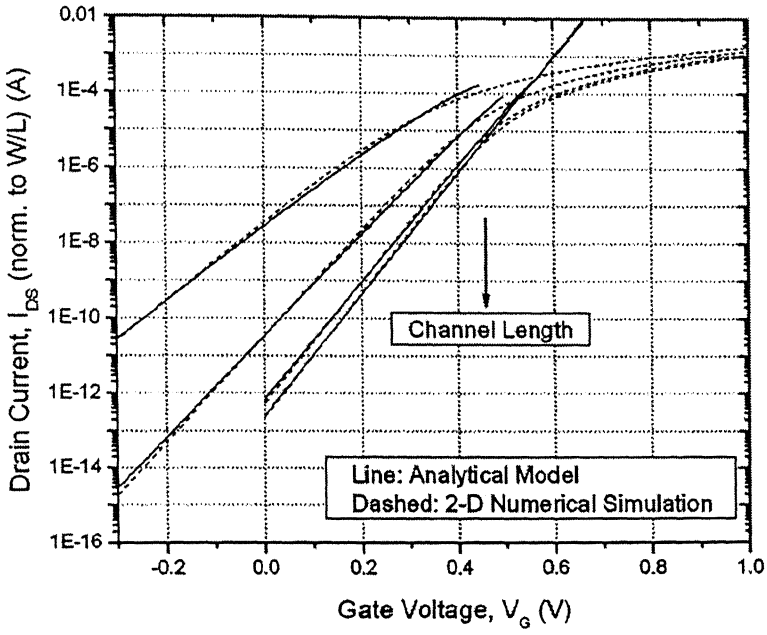

Figure 3.2. Comparison of analytical current model Eq. (3.15) with 2-D atlas simulation for varying lengths. V_{DS}=1.0 V, t_{si} = 10 nm, t_{ox} = 1.2 nm, L = 20, 30, 50 and 70 nm, $V_{FB,f} = V_{FB,b}$ = 0 V, mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$

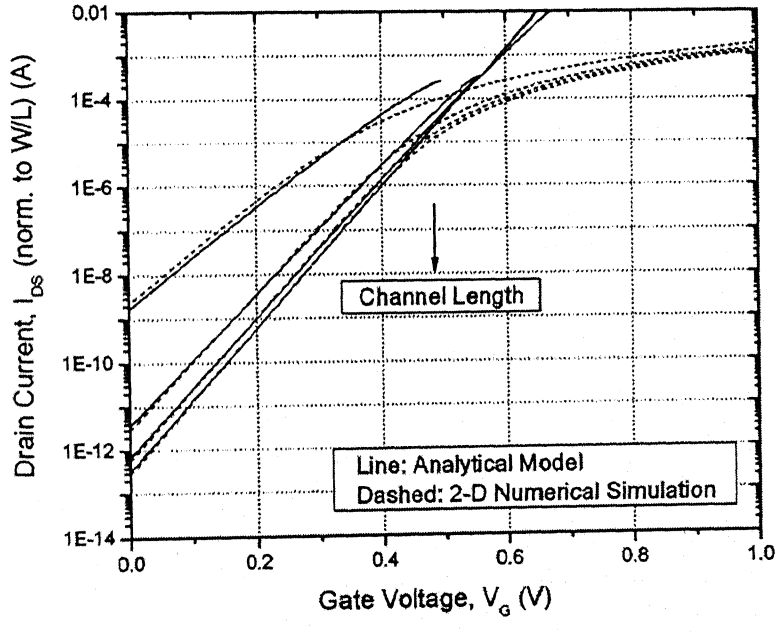

Figure 3.3. Comparison of analytical current model Eq. (3.15) with 2-D atlas simulation for varying lengths. V_{DS}=1.0 V, t_{si} = 15 nm, t_{ox} = 1.0 nm, L = 30, 50, 70 and 100 nm, $V_{FB,f} = V_{FB,b}$ = 0 V, mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$

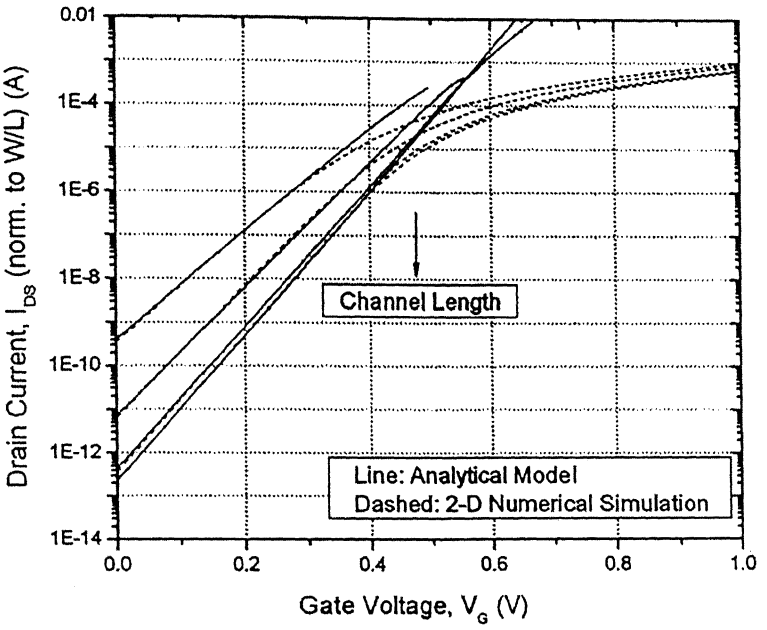

Figure 3.4. Comparison of analytical current model Eq. (3.15) with 2-D atlas simulation for varying lengths. V_{DS}=1.0 V, t_{si} = 20 nm, t_{ox} = 2.0 nm, L = 50, 70, 150 and 300 nm, $V_{FB,f} = V_{FB,b} = 0$ V , mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$

3.5.2 Sub-threshold Slope Comparison Results

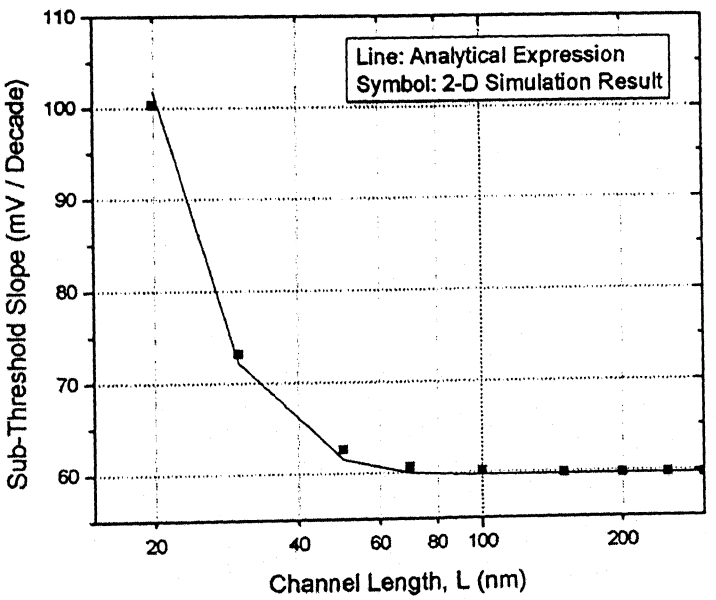

Figure 3.5. Comparison of analytical sub-threshold slope model Eq. (3.19) with 2-D atlas simulation for varying lengths. V_{DS}=1.0 V, t_{si} = 10 nm, t_{ox} = 1.5 nm, L = 20, 30, 50, 70, 100, 150, 200, 250 and 300 nm, $V_{FB,f} = V_{FB,b} = 0$ V , mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$

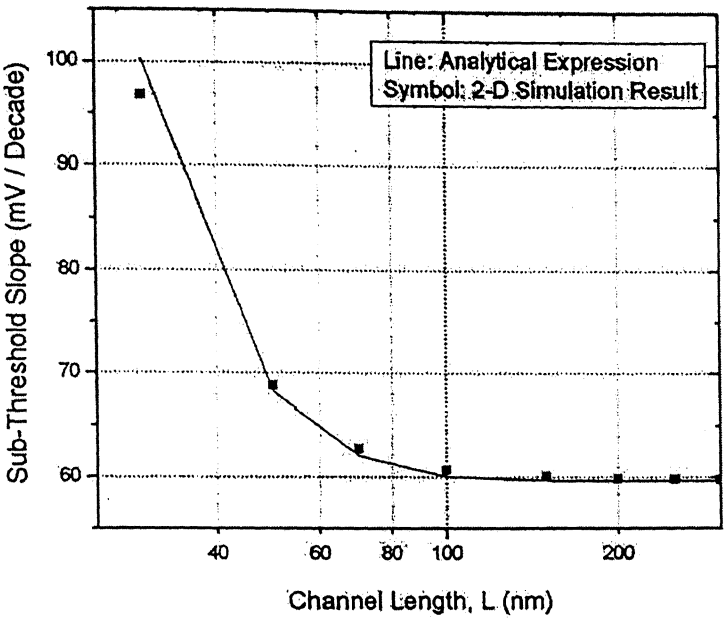

Figure 3.6. Comparison of analytical sub-threshold slope model Eq. (3.19) with 2-D atlas simulation for varying lengths. V_{DS}=1.0 V, t_{si} = 15 nm, t_{ox} = 2.0 nm, L = 30, 50, 70, 100, 150, 200, 250 and 300 nm, $V_{FB,f} = V_{FB,b}$ = 0 V , mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$

Figure 3.5 and figure 3.6 show the comparison of sub-threshold slope values obtained using Eq. (3.19) and those extracted from 2-D Atlas simulation. A good agreement is found between the two showing the validity of Eq. (3.19).

3.5.3 Threshold Voltage Roll-off Comparison

For comparison of threshold voltage roll-off, the most widely used definition of threshold voltage based on constant current is used. As is mentioned in Arora [17], current can be chosen between 10^{-9}-10^{-6} A after normalizing it with W/L. In present work, the current level is taken as 10^{-8} A. Thus threshold voltage is calculated for different lengths at the points where I_{DS} = W/L*10^{-8} A. For calculating threshold voltage roll-off, the longest channel threshold voltage is considered as the reference and the decrease in threshold voltage for smaller lengths is calculated with respect to this long channel threshold voltage. A good agreement is found between the roll-offs obtained using analytical model results and 2-D simulations results. Along with this the effect of drain voltage on roll-off is also studied. The results of comparisons are shown in figures 3.7- 3.10 below.

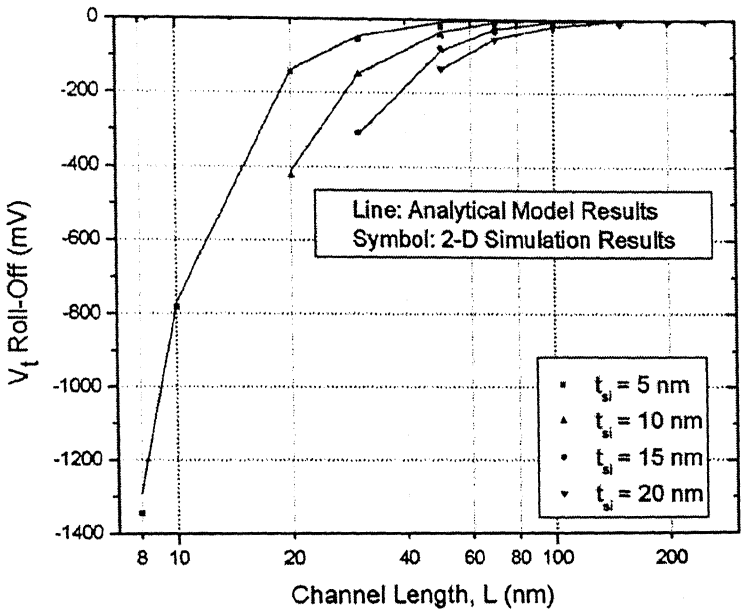

Figure 3.7. Comparison of threshold voltage roll-off obtained from analytical model Eq. (3.15) with 2-D atlas simulation for varying silicon body thickess. V_{DS}=1.0 V, t_{ox} = 1.5 nm, L = 8, 10, 20, 30, 50, 70, 100, 150, 200, 250 and 300 nm, $V_{FB,f} = V_{FB,b} = 0$ V , mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$

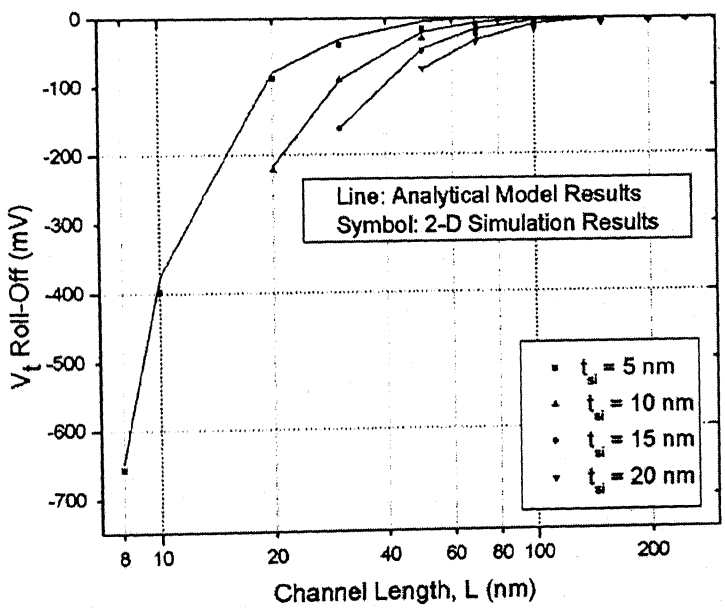

Figure 3.8. Comparison of threshold voltage roll-off obtained from analytical model Eq. (3.15) with 2-D atlas simulation for varying silicon body thickess. V_{DS}=0.01 V, t_{ox} = 2.0 nm, L = 8, 10, 20, 30, 50, 70, 100, 150, 200, 250 and 300 nm, $V_{FB,f} = V_{FB,b} = 0$ V , mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$

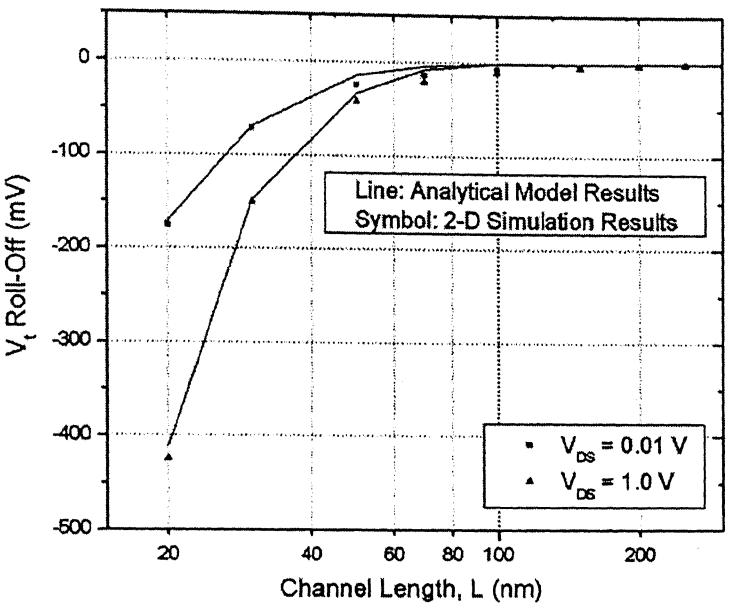

Figure 3.9 Comparison of threshold voltage roll-off obtained from analytical model Eq. (3.15) with 2-D atlas simulation for varying drain bias, showing effect of DBL. t_{si} = 10 nm, t_{ox} = 1.5 nm, L = 20, 30, 50, 70, 100, 150, 200, 250 and 300 nm, $V_{FB,f} = V_{FB,b} = 0$ V, mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$

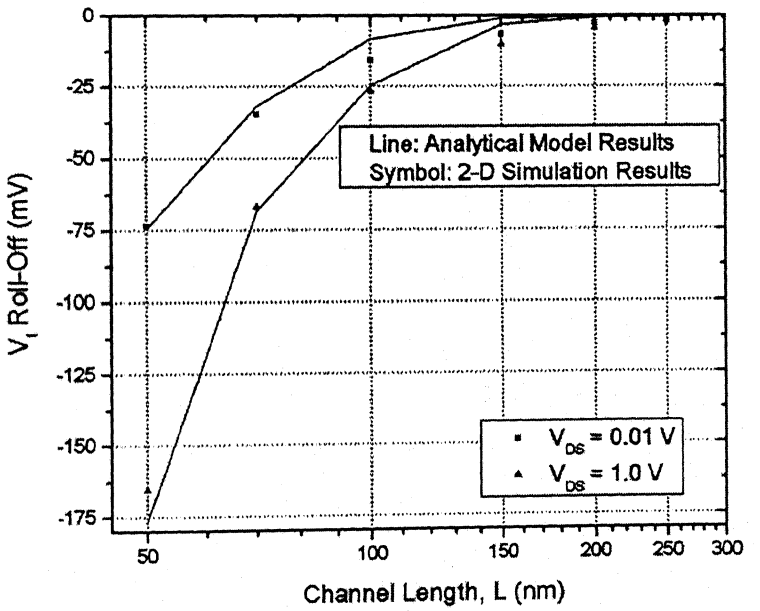

Figure 3.10. Comparison of threshold voltage roll-off obtained from analytical model Eq. (3.15) with 2-D atlas simulation for varying drain bias, showing effect of DBL. t_{si} = 20 nm, t_{ox} = 2.0 nm, L = 50, 70, 100, 150, 200, 250 and 300 nm, $V_{FB,f} = V_{FB,b} = 0$ V, mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$

Chapter 4

Modeling of Surface-Potential for Asymmetric DG MOSFET along the channel in the Sub-Threshold Region using Gauss's Law

4.1 Gauss Law

The asymmetric device that is considered in this work is operated in asymmetric mode by varying the work function of the top and bottom gates. The mode of operation of the device is as illustrated in figure 4.1 below with top gate as n+ poly-silicon $\left(V_{Fb,f} = -0.56V\right)$ and bottom gate as p+ poly-silicon $\left(V_{Fb,b} = 0.56V\right)$.

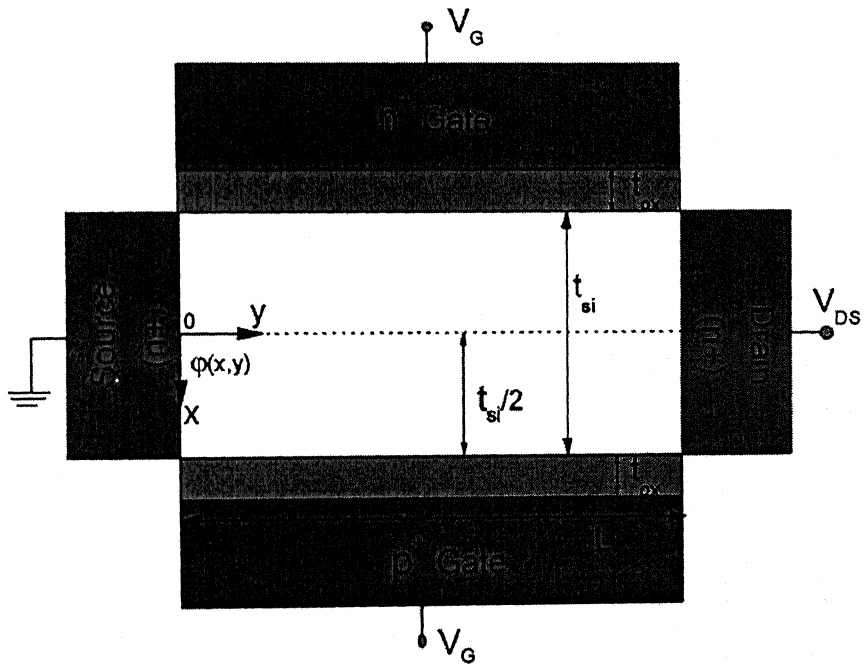

Figure 4.1. Asymmetric DG MOSFET Structure

In the device, the same gate voltage is applied to both the gates and the same oxide thickness is kept for top and bottom gate. Applying the Gauss's law to the silicon body of the asymmetric DG MOSFET

$$-\varepsilon_{si}\int_{-t_{si}/2}^{t_{si}/2}\frac{\partial\varphi(x,y)}{\partial y}\,dx-\varepsilon_{ox}\int_{0}^{y}E_{ox,f}(y')\,dy'-\varepsilon_{ox}\int_{0}^{y}E_{ox,b}(y')\,dy'=Q_i\,t_{si}\,y \qquad (4.1)$$

where the first term on the L.H.S represents the net electric flux entering the silicon body from the lateral direction and the second and the third term represents the net

electric flux entering the body from the top and bottom. The R.H.S represents the net charge enclosed by the Gaussian box.

In case of sub-threshold region, the mobile charge carriers will be neglected. Thus Eq. (4.1) becomes

$$-\varepsilon_{si}\int_{-t_{si}/2}^{t_{si}/2}\frac{\partial\varphi(x,y)}{\partial y}\,dx-\varepsilon_{ox}\int_{0}^{y}E_{ox,f}(y')\,dy'-\varepsilon_{ox}\int_{0}^{y}E_{ox,b}(y')\,dy'=0 \qquad (4.2)$$

4.2 Assumption for potential variation in perpendicular direction

It has been shown in the earlier works of Yuan Taur [16] and Gen pei et. al [7] and also verified by 2-D Atlas simulations that in the sub-threshold region, potential variation along the perpendicular direction (i.e. x-direction) is linear. One of the plots showing the variation of potential along x-direction is shown in figure 4.2 below.

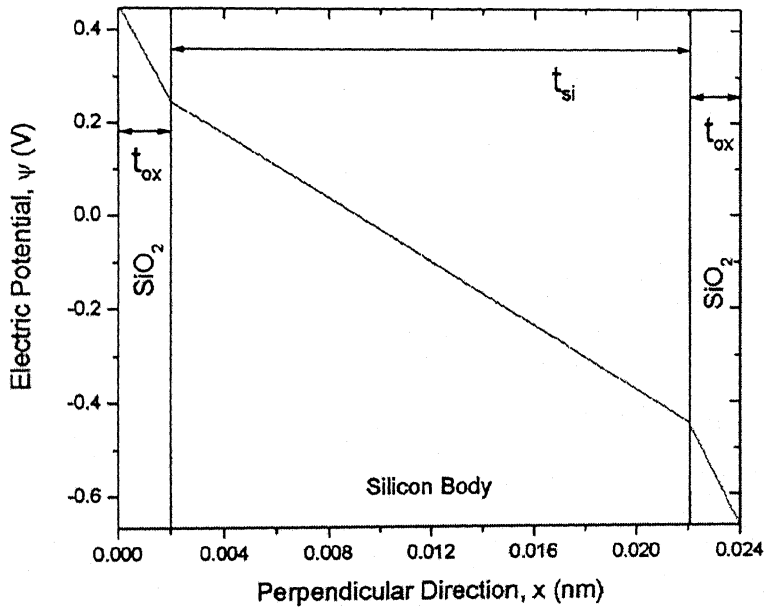

Figure 4.2. Variation of potential perpendicular to channel. t_{si} = 20 nm, t_{ox} = 2.0 nm, V_G = 0.1 V, V_{DS} = 1.5 V, L=300 nm. (Simulation done using Atlas)

Thus one can assume potential to be varying linearly along the perpendicular direction and can be written as

$$\varphi(x,y) = k_1 x + k_2 \tag{4.3}$$

with the following boundary conditions

$$\varphi\left(-\frac{t_{si}}{2}, y\right) = \varphi_{s,f}(y) \text{ = Front-Gate surface potential} \tag{4.4}$$

$$\varphi\left(\frac{t_{si}}{2}, y\right) = \varphi_{s,b}(y) \text{= Back-Gate surface potential} \tag{4.5}$$

Based on Eq. (4.4) and Eq. (4.5) it can be shown that $\varphi(x,y)$ is given by

$$\varphi(x,y) = \frac{(\varphi_{s,b} - \varphi_{s,f})}{t_{si}} x + \frac{(\varphi_{s,b} + \varphi_{s,f})}{2} \tag{4.6}$$

Differentiating Eq. (4.6) with respect to y one gets

$$\frac{\partial \varphi(x,y)}{\partial y} = \frac{x}{t_{si}}\left(\frac{\partial \varphi_{s,b}(y)}{\partial y} - \frac{\partial \varphi_{s,f}(y)}{\partial y}\right) + \frac{1}{2}\left(\frac{\partial \varphi_{s,b}(y)}{\partial y} + \frac{\partial \varphi_{s,f}(y)}{\partial y}\right) \tag{4.7}$$

Integrating Eq. (4.7) from $-t_{si}/2$ to $t_{si}/2$

$$\int_{-t_{si}/2}^{t_{si}/2} \frac{\partial \varphi(x,y)}{\partial y} dx = \frac{1}{t_{si}}\left(\frac{\partial \varphi_{s,b}(y)}{\partial y} - \frac{\partial \varphi_{s,f}(y)}{\partial y}\right) \int_{-t_{si}/2}^{t_{si}/2} x\, dx + \frac{1}{2}\left(\frac{\partial \varphi_{s,b}(y)}{\partial y} + \frac{\partial \varphi_{s,f}(y)}{\partial y}\right) \int_{-t_{si}/2}^{t_{si}/2} dx$$

$$= \frac{1}{t_{si}}\left(\frac{\partial \varphi_{s,b}(y)}{\partial y} - \frac{\partial \varphi_{s,f}(y)}{\partial y}\right) \left|\frac{x^2}{2}\right|_{-t_{si}/2}^{t_{si}/2} + \frac{1}{2}\left(\frac{\partial \varphi_{s,b}(y)}{\partial y} + \frac{\partial \varphi_{s,f}(y)}{\partial y}\right) t_{si}$$

$$= \frac{t_{si}}{2}\left(\frac{\partial \varphi_{s,b}(y)}{\partial y} + \frac{\partial \varphi_{s,f}(y)}{\partial y}\right) \tag{4.8}$$

As mentioned earlier that for short-channel device, potential no longer varies linearly in the x-direction. Thus parameter η [†] is introduced to adjust the lateral flux for short channel devices. Eq. (4.8) is then modified to

$$\int_{-t_{si}/2}^{t_{si}/2} \frac{\partial \varphi(x,y)}{\partial y} dx = \frac{t_{si}}{2\eta}\left(\frac{\partial \varphi_{s,b}(y)}{\partial y} + \frac{\partial \varphi_{s,f}(y)}{\partial y}\right) \tag{4.9}$$

Eq. (4.2) and Eq. (4.9) give

$$\frac{\varepsilon_{si} t_{si}}{2\eta}\left[\frac{\partial \varphi_{s,b}}{\partial y} + \frac{\partial \varphi_{s,f}}{\partial y}\right] + \varepsilon_{ox} \int_0^y E_{ox,f}(y')\, dy' + \varepsilon_{ox} \int_0^y E_{ox,b}(y')\, dy' = 0 \tag{4.10}$$

[†] *Refer section 5.4.1*

Now $E_{ox,f}(y')$ and $E_{ox,b}(y')$ are the fields entering from the top and bottom gates and are given by

$$E_{ox,f}(y)=\frac{\left[V_G-V_{FB,f}-\varphi_{s,f}(y)\right]}{t_{ox}} \tag{4.11}$$

$$E_{ox,b}(y)=\frac{\left[V_G-V_{FB,b}-\varphi_{s,b}(y)\right]}{t_{ox}} \tag{4.12}$$

Putting Eq. (4.11) and Eq. (4.12) in Eq. (4.10) and differentiating with respect to y

$$\frac{\varepsilon_{si}t_{si}}{2\eta}\left[\frac{d^2\varphi_{s,b}(y)}{dy^2}+\frac{d^2\varphi_{s,f}(y)}{dy^2}\right]+\frac{\varepsilon_{ox}}{t_{ox}}\left[V_G-V_{FB,f}-\varphi_{s,f}(y)\right]+\frac{\varepsilon_{ox}}{t_{ox}}\left[V_G-V_{FB,b}-\varphi_{s,b}(y)\right]=0 \tag{4.13}$$

Now, by solving 1-D Poisson's equation one can get, [13]

$$\begin{aligned}\varphi_{s,b} &= \varphi_{s,f}-E_{s,f}\,t_{si}=\varphi_{s,f}-\frac{C_{ox}}{C_{si}}\left(V_G-V_{FB,f}-\varphi_{s,f}\right)\\ &=\varphi_{s,f}\left(1+\frac{C_{ox}}{C_{si}}\right)-\frac{C_{ox}}{C_{si}}\left(V_G-V_{FB,f}\right)\end{aligned} \tag{4.14}$$

From Eq. (4.14) one gets

$$\frac{d^2\varphi_{s,b}}{dy^2}=\frac{d^2\varphi_{s,f}}{dy^2}\left(1+\frac{C_{ox}}{C_{si}}\right) \tag{4.15}$$

Using Eq. (4.14) and Eq. (4.15) in Eq. (4.13) one obtains

$$\frac{d^2\varphi_{s,f}(y)}{dy^2}=\frac{1}{\lambda^2}\left[\varphi_{s,f}(y)-V_{Geff,f}\right] \tag{4.16}$$

where $\lambda=\sqrt{\frac{\varepsilon_{si}t_{si}t_{ox}}{2\eta\varepsilon_{ox}}}\equiv Characteristic\ Length$,

$V_{Geff,f}=V_G-\alpha V_{FB,f}-(1-\alpha)V_{FB,b}$, and

$$\alpha=\left(\frac{1+\frac{C_{ox}}{C_{si}}}{2+\frac{C_{ox}}{C_{si}}}\right)\equiv Gate\ coupling\ factor$$

4.3 Formulation of boundary Conditions

Now to formulate the boundary conditions an undoped body DG MOSFET is assumed with n+ source and drain.

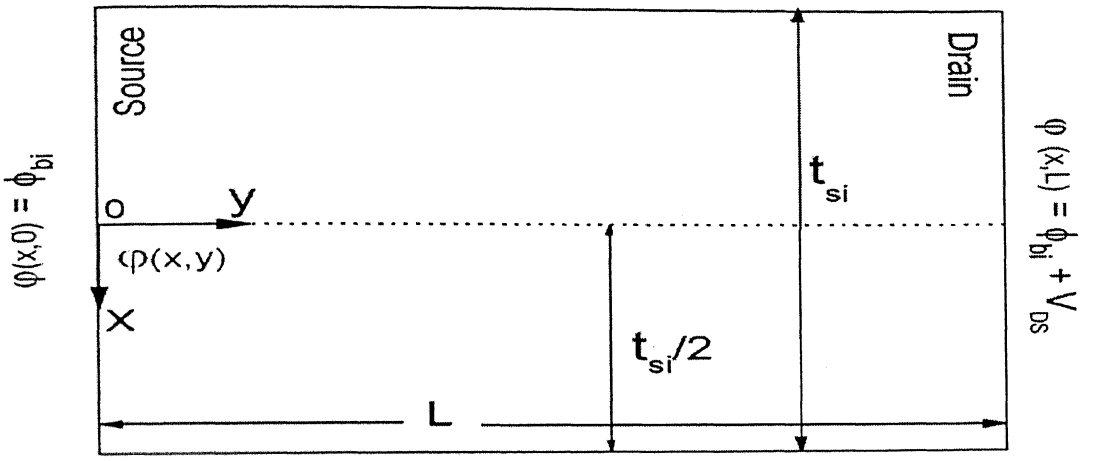

Figure 4.3. Boundary conditions for potential at various surfaces of the silicon body for asymmetric DG MOSFET

The boundary conditions, as shown in figure 4.3, are

$$\varphi_{s,f}(0) = \varphi(-\frac{t_{si}}{2}, 0) = \phi_{bi} \quad \text{(I)}$$

$$\varphi_{s,f}(L) = \varphi(-\frac{t_{si}}{2}, L) = \phi_{bi} + V_{DS} \quad \text{(II)}$$

$$\varphi_{s,b}(0) = \varphi(\frac{t_{si}}{2}, 0) = \phi_{bi} \quad \text{(III)}$$

$$\varphi_{s,b}(L) = \varphi(\frac{t_{si}}{2}, L) = \phi_{bi} + V_{DS} \quad \text{(IV)}$$

4.4 Analytical Model for Surface Potential in Sub-threshold Region

Eq. (4.16) is same as Eq. (2.8) with similar boundary condition. It is solved using boundary conditions (I) and (II) as is done for Eq. (2.8) in appendix B to give the following expression for the front gate surface potential along the channel in the sub-threshold region

$$\varphi_{s,f}(y) = V_{Geff,f} + \left(\varphi_{s,f}(0) - V_{Geff,f}\right)\left(\frac{\sinh\left(\frac{L-y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}\right) + \left(\varphi_{s,f}(L) - V_{Geff,f}\right)\left(\frac{\sinh\left(\frac{y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}\right) \quad (4.17)$$

Similar expression for back gate surface potential along the channel can be found as given in Eq. (4.18) below

$$\varphi_{s,b}(y) = V_{Geff,b} + \left(\varphi_{s,b}(0) - V_{Geff,b}\right)\left(\frac{\sinh\left(\frac{L-y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}\right) + \left(\varphi_{s,b}(L) - V_{Geff,b}\right)\left(\frac{\sinh\left(\frac{y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}\right) \quad (4.18)$$

where $V_{Geff,b} = V_G - \alpha V_{FB,b} - (1-\alpha)V_{FB,f}$

From Eq. (4.17) and Eq. (4.18) it is clear that both front gate surface potential and back gate surface potential show similar behaviour as shown by surface potential along channel for symmetric DG MOSFET case. Figure 4.4 and figure 4.5 show the calculated results based upon Eq. (4.17) and Eq. (4.18) along with its comparison with the 2-D numerical simulations obtained using Atlas device simulator for small drain bias.

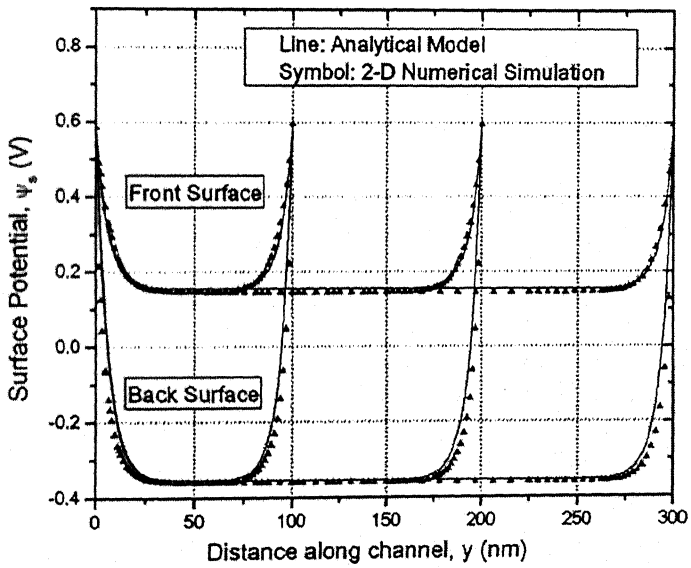

Figure 4.4. Comparison of Surface Potential along channel for analytical model Eq. (4.17) and Eq. (4.18) with 2-D Numerical Simulation (longer lengths) for small drain bias (V_{DS} = 0.01 V), t_{ox} = 2.0 nm, t_{si} = 10 nm, V_G = -0.1 V, $V_{FB,f}$ = -0.56 V, $V_{FB,b}$ = 0.56 V, L=100, 150 and 300 nm.

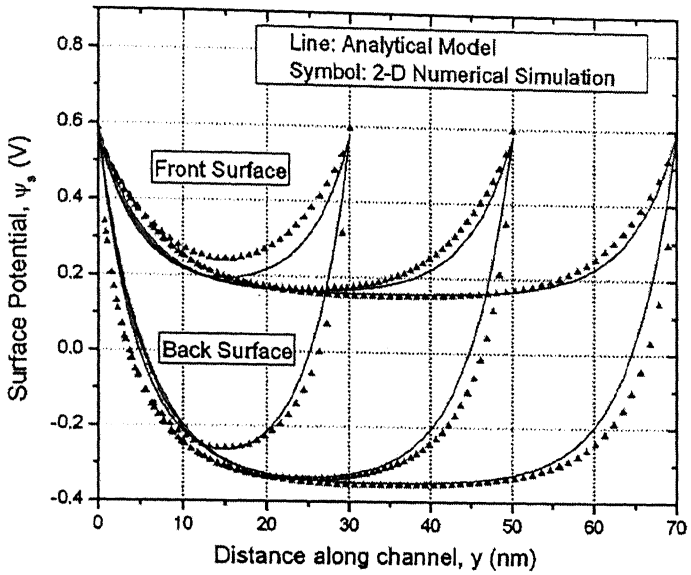

Figure 4.5. Comparison of Surface Potential along channel for analytical model Eq. (4.17) and Eq. (4.18) with 2-D Numerical Simulation (short lengths) for small drain bias (V_{DS} = 0.01 V), t_{ox} = 2.0 nm, t_{si} = 10 nm, V_G = -0.1 V, $V_{FB,f}$ = -0.56 V, $V_{FB,b}$ = 0.56 V, L=30, 50 and 70 nm

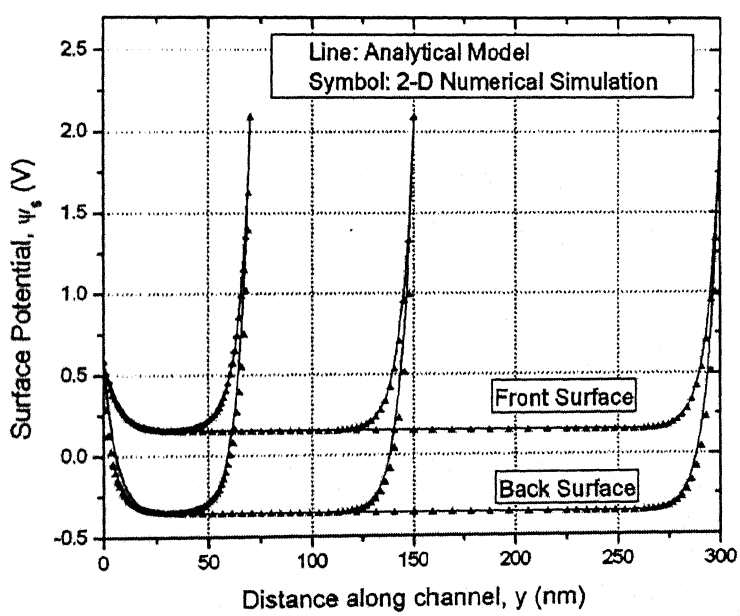

Figure 4.6. Comparison of Surface Potential along channel for analytical model Eq. (4.17) and Eq. (4.18) with 2-D Numerical Simulation (longer lengths) for large drain bias (VDS = 1.5 V), tox = 2.0 nm, tsi = 10 nm, VG = -0.1 V, VFB,f = -0.56 V, VFB,b = 0.56 V, L=70, 150 and 300 nm.

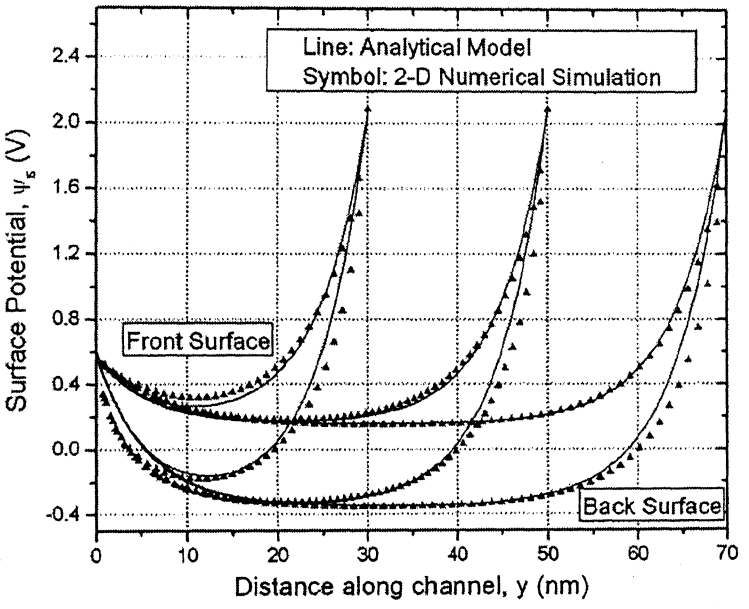

Figure 4.7. Comparison of Surface Potential along channel for analytical model Eq. (4.17) and Eq. (4.18) with 2-D Numerical Simulation (short lengths) for large drain bias (V_{DS} = 1.5 V), t_{ox} = 2.0 nm, t_{si} = 10 nm, V_G = -0.1 V, $V_{FB,f}$ = -0.56 V, $V_{FB,b}$ = 0.56 V, L=30, 50 and 70 nm.

From figure 4.4 and figure 4.5 it is clear that potential shows behaviour similar to symmetric DG MSOFET. As the channel length is decreased, potential no longer remains constant along the channel. Figure 4.6 and figure 4.7 show the variation of surface potential along the channel for larger values of drain voltage indicating the validity of the model for higher values of V_{DS} also.

Chapter 5

Modeling of Sub-Threshold Current

In chapter 3 it was discussed that in sub-threshold region the current is mainly due to diffusion so only diffusion component of current will be considered for formulation of the model.

5.1 Diffusion current

Sub-threshold current densities can be expressed as

$$J_n = J_{n,diff} \tag{5.1}$$

$$J_p = J_{p,diff} \tag{5.2}$$

Since an n-DG MOSFET is considered so the current due to electrons will be calculated. Diffusion current is given by

$$J_{n,diff} = qD_n \frac{dn}{dy} \tag{5.3}$$

From Eq. (5.3) the expression for sub-threshold current is given by

$$I_{DS} = qD_n W \left(\int_{-t_{si}/2}^{t_{si}/2} \frac{dn(x,y)}{dy} dx \right) = qD_n W \left(\int_{-t_{si}/2}^{t_{si}/2} \frac{dn(x,y)}{dV_{channel}} \frac{dV_{channel}}{dy} dx \right)$$

$$= qD_n W \frac{dV_{channel}}{dy} \left(\int_{-t_{si}/2}^{t_{si}/2} \frac{dn(x,y)}{dV_{channel}} dx \right) \tag{5.4}$$

where $V_{channel}$ is the potential variation along channel direction due to applied drain bias and is a function of y only.

Mobile charge expression is given by

$$n(x,y) = n_i \exp\left(\frac{\varphi(x,y) - V_{channel}(y)}{\phi_t} \right) \tag{5.5}$$

Thus one gets,

$$\frac{d\,n(x,y)}{dV_{channel}} = n_i \exp\left(\frac{\varphi(x,y) - V_{channel}(y)}{\phi_t} \right) \left(\frac{-1}{\phi_t} \right) = n(x,y) \left(\frac{-1}{\phi_t} \right) \tag{5.6}$$

Using Eq. (5.6) in Eq. (5.4) one gets,

$$I_{DS} = qD_n W \left(\frac{-1}{\phi_t} \right) \frac{dV_{channel}}{dy} \left(\int_{-t_{si}/2}^{t_{si}/2} n(x,y)\,dx \right) = qD_n W \left(\frac{-1}{\phi_t} \right) n(y) \frac{dV_{channel}}{dy} \tag{5.7}$$

Evaluation of $n(y)$ is done by integrating Eq. (5.5) from the top surface to the bottom of silicon body (Appendix D)

$$n(y) = n_i t_{si} \frac{\left[\exp\left(\frac{\varphi_{s,b}}{\phi_t}\right) - \exp\left(\frac{\varphi_{s,f}}{\phi_t}\right)\right]}{\left[\left(\frac{\varphi_{s,b}}{\phi_t}\right) - \left(\frac{\varphi_{s,f}}{\phi_t}\right)\right]} \exp\left(\frac{-V_{channel}(y)}{\phi_t}\right) = \frac{n_i t_{si}}{\Re(y)} \exp\left(\frac{-V_{channel}(y)}{\phi_t}\right) \tag{5.8}$$

where

$$\Re(y) = \frac{\left[\left(\frac{\varphi_{s,b}}{\phi_t}\right) - \left(\frac{\varphi_{s,f}}{\phi_t}\right)\right]}{\left[\exp\left(\frac{\varphi_{s,b}}{\phi_t}\right) - \exp\left(\frac{\varphi_{s,f}}{\phi_t}\right)\right]}$$

Thus using Eq. (5.8) in Eq. (5.7) one gets

$$I_{DS} = qD_n W \left(\frac{-1}{\phi_t}\right) \frac{n_i t_{si}}{\Re(y)} \exp\left(\frac{-V_{channel}(y)}{\phi_t}\right) \frac{dV_{channel}}{dy} \tag{5.9}$$

Integrating from source to drain gives

$$I_{DS} = qn_i D_n W t_{si} \left[1 - \exp\left(\frac{-V_{DS}}{\phi_t}\right)\right] \Big/ \int_0^L \Re(y)\, dy \tag{5.10}$$

Also Einstein's relation relates diffusion coefficient to the mobility as follows

$$D_n = \phi_t \mu_n \tag{5.11}$$

Thus expression for sub-threshold current becomes

$$I_{DS} = qn_i \mu_n \phi_t W t_{si} \left[1 - \exp\left(\frac{-V_{DS}}{\phi_t}\right)\right] \Big/ \int_0^L \Re(y)\, dy \tag{5.12}$$

From Eq. (5.12) it is clear that it can not be solved analytically. So we need to come up with some constant K such that the integral in the denominator of Eq. (5.12) can be written as

$$\int_0^L \Re(y)\, dy = K \int_0^L dy = K.L \tag{5.13}$$

K is nothing but the average value of integral over the range of integration. Thus, if one can come up with some analytical expression for K then Eq. (5.12) can be converted into an analytical expression.

5.2 Evaluation of Integral K

Function $\Re(y)$ is plotted in figure 5.11. The average value (K) of $\Re(y)$ is calculated numerically. Also plotted in the figure is the back surface potential as a function of y.

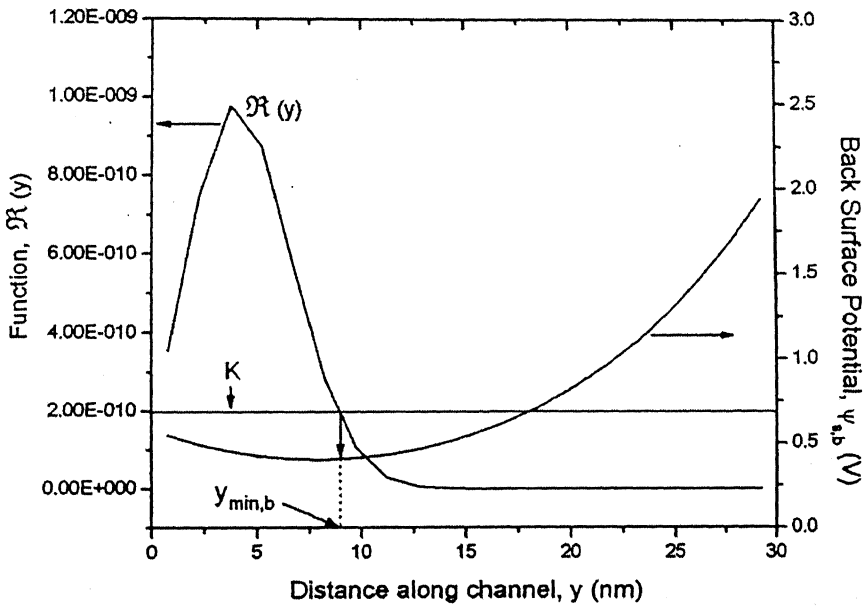

Figure 5.1. Comparison of $\Re(y)$ with back surface potential along the channel. t_{si} = 10 nm, t_{ox} = 1.5 nm, V_G = -0.1 V, V_{DS} = 1.5 V, L = 30 nm, $V_{FB,f}$ = -0.56 V, $V_{FB,b}$ = 0.56 V.

From the figure it is clear that the average value of $\Re(y)$ is occurring close to the point of minimum back surface potential ($y_{\min,b}$). So if one evaluates the function under integral at the point where the minimum of back surface potential is occurring then a reasonable value of K can be obtained. Based on this assumption, K can be represented as

$$K = \left.\frac{\left[\left(\frac{\varphi_{s,b}}{\phi_t}\right) - \left(\frac{\varphi_{s,f}}{\phi_t}\right)\right]}{\left[\exp\left(\frac{\varphi_{s,b}}{\phi_t}\right) - \exp\left(\frac{\varphi_{s,f}}{\phi_t}\right)\right]}\right|_{y=y_{\min,b}} \tag{5.14}$$

where $y_{\min,b}$ is the point along channel where the back surface potential is minimum. Now $y_{\min,b}$ can be found using the similar procedure as applied for symmetric case for finding out the minimum surface potential point. From the procedure outlined in appendix C one gets the following expression for $y_{\min,b}$

$$y_{\min,b} = \frac{\lambda}{2}\ln\left[\frac{\left(\varphi_{s,b}(0)-V_{Geff,b}\right)\exp\left(\frac{L}{\lambda}\right)-\left(\varphi_{s,b}(L)-V_{Geff,b}\right)}{\left(\varphi_{s,b}(L)-V_{Geff,b}\right)-\left(\varphi_{s,b}(0)-V_{Geff,b}\right)\exp\left(\frac{-L}{\lambda}\right)}\right] \tag{5.15}$$

From Eq. (5.12), Eq. (5.14) and Eq. (5.15), the final analytical expression for sub-threshold current can be written as

$$I_{DS} = qn_i\mu_n\phi_t\frac{W}{K.L}t_{si}\left[1-\exp\left(\frac{-V_{DS}}{\phi_t}\right)\right] \tag{5.16}$$

5.3 Sub-threshold Swing Formulation

As mentioned in chapter 3, sub-threshold swing is an important performance measurement parameter for a MOSFET in sub-threshold region. Sub-threshold swing is given by

$$S = \left[\frac{d(\log I_{DS})}{dV_G}\right]^{-1} = 2.303\left[\frac{d(\ln I_{DS})}{dV_G}\right]^{-1} \qquad (V\ /\ decade) \tag{5.17}$$

Now from Eq. (5.16)

$$\frac{d(\ln I_{DS})}{dV_G} = -\frac{d\ln K}{dV_G} = -\frac{1}{K}\frac{dK}{dV_G} \tag{5.18}$$

Using Eq. (5.14) one gets

$$\frac{d(\ln I_{DS})}{dV_G} = \frac{1}{\phi_t}\left[1-\frac{\sinh\left(\frac{L-y_{\min,b}}{\lambda}\right)+\sinh\left(\frac{y_{\min,b}}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}\right] \tag{5.19}$$

The mathematical analysis done to obtain Eq. (5.19) is shown in appendix E. Thus final sub-threshold slope expression for asymmetric DG MOSFET is given as

$$S = 2.303\phi_t \left[1 - \frac{\sinh\left(\frac{L - y_{min,b}}{\lambda}\right) + \sinh\left(\frac{y_{min,b}}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)} \right]^{-1} \tag{5.20}$$

In Eq. (5.20) it can be seen that the sub-threshold swing is dependent upon V_G through $y_{min,b}$. So to make sure that device is well within sub-threshold region and for comparison with the results obtained with 2-dimensional device simulation, V_G is kept as $-5\phi_t$.

5.4 Results of comparison with 2-D numerical simulation

The basic device structure shown in chapter 4 is made in 2-D device simulator and simulated using Atlas. Results have been verified by varying channel length from 300 nm down to 20 nm, silicon thickness from 5 nm to 20 nm in steps of 5 nm and for 4 oxide thickness values of 1.0 nm, 1.2 nm, 1.5 nm and 2.0 nm. Along with that constant mobility model is used with mobility value of 1400 $cm^2V^{-1}sec^{-1}$.

From figures 4.4 – 4.7 one can see that surface potential is not exactly matching with the 2-D simulation results. But as far as predicting the value of K is concerned, the proposed model is able to predict it within reasonable error range compared to 2-D simulation results as shown in figure 5.2. The squares in the figure show the error f_e as a function of y where f_e is given by

$$f_e = \left(\frac{\Re(y)\big|_{2-D} - \Re(y)\big|_{analytical}}{\Re(y)\big|_{2-D}} \right) x100 \tag{5.21}$$

Also is shown the variation of back surface potential along the channel. The back surface potential is calculated using the analytical expression using Eq. (4.18).

From the figure it is clear that the percentage error in evaluation of value of $\Re(y)$ is minimum in the region close to $y_{min,b}$ as is outlined by the box in figure 5.2. Now K is evaluated at $y_{min,b}$. This explains why the approximation gives a reasonable match of model with the 2-D simulation results as shown in following sub-sections.

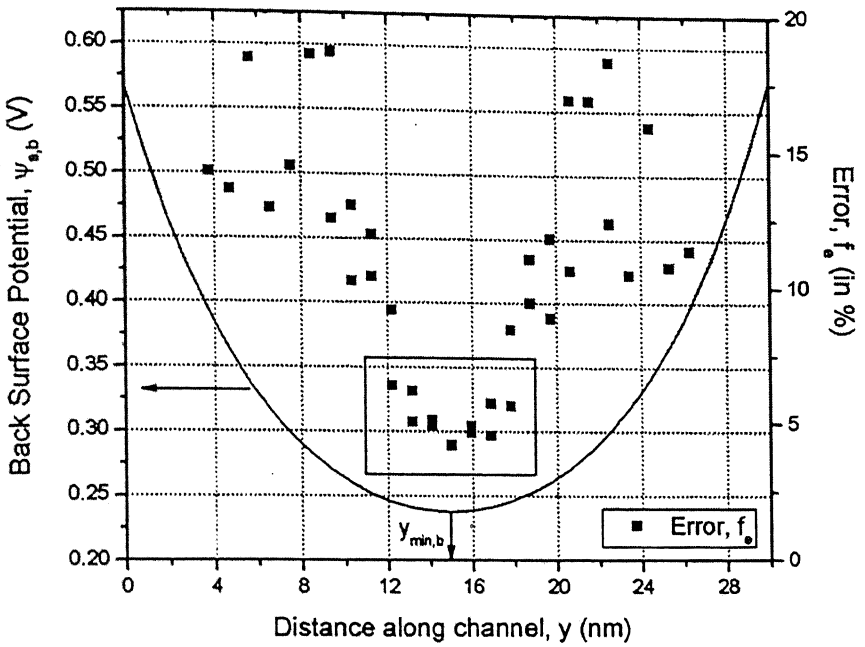

Figure 5.2. Variation of percentage error f_e along the channel. V_{DS} = 0.01 V, t_{ox} = 2.0 nm, t_{si} = 10 nm, V_G = -0.1 V, $V_{FB,f}$ = -0.56 V, $V_{FB,b}$ = 0.56 V, L=30 nm.

5.4.1 Current Comparison Results

Figures 5.3 – 5.6 show the comparison of model results with numerical simulations for different oxide thickness and silicon body thickness. Now due to simplicity of model and the simplifying assumptions made in formulations of the model, the maximum error in predicting current values have been under 50%. Similar to what has been done for symmetric case, the expression of parameter η found using exponential regression analysis with COD value of 0.952, is given as

$$\eta = e^{(2.01028)} t_{si}^{(0.33548)} t_{ox}^{(0.99581)} L^{(-1.07241)} \tag{5.22}$$

where t_{si}, t_{ox} and L are in nm.

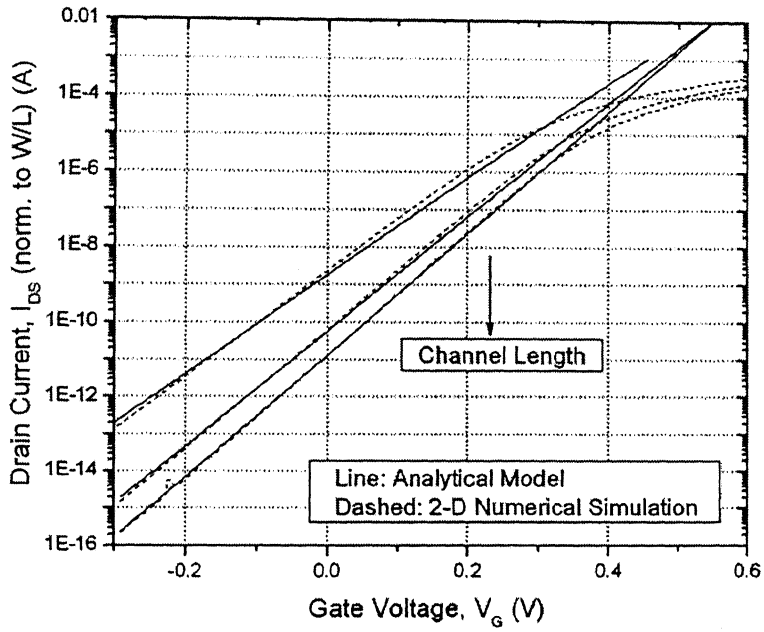

Figure 5.3. Comparison of analytical current model Eq. (5.16) with 2-D atlas simulation for varying lengths. V_{DS}=1.0 V, t_{si} = 5 nm, t_{ox} = 1.5 nm, L = 20, 30 and 50 nm, $V_{FB,f}$ = -0.56 V, $V_{FB,b}$ = 0.56 V, mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$

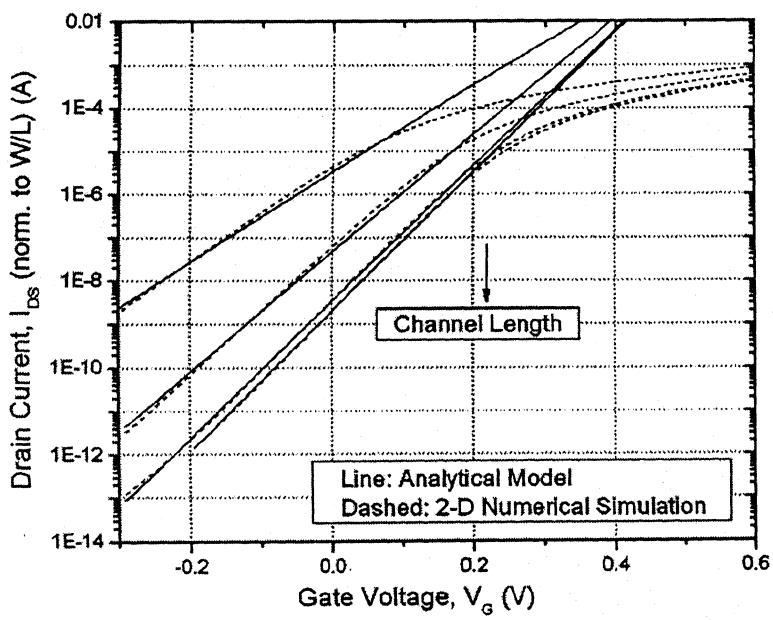

Figure 5.4. Comparison of analytical current model Eq. (5.16) with 2-D atlas simulation for varying lengths. V_{DS}=1.0 V, t_{si} = 10 nm, t_{ox} = 1.2 nm, L = 20, 30, 50 and 70 nm, $V_{FB,f}$ = -0.56 V, $V_{FB,b}$ = 0.56 V, mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$

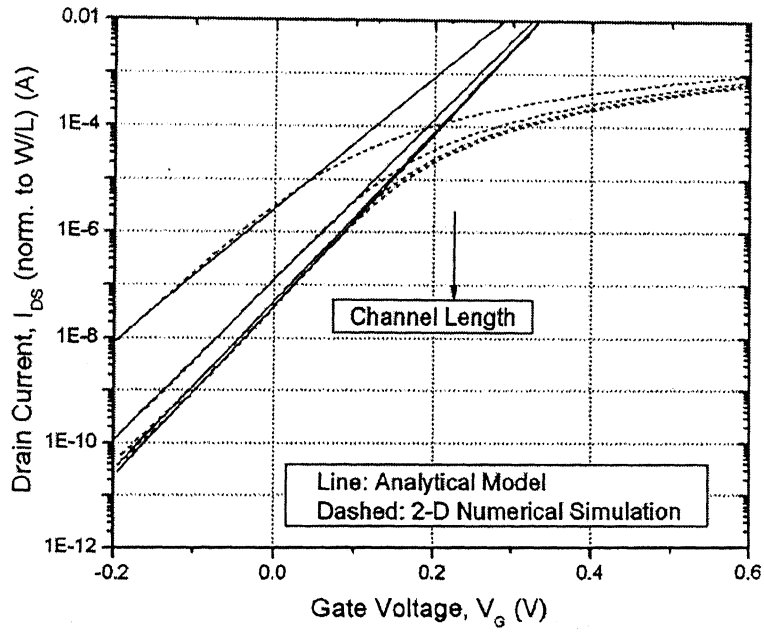

Figure 5.5. Comparison of analytical current model Eq. (5.16) with 2-D atlas simulation for varying lengths. V_{DS}=1.0 V, t_{si} = 15 nm, t_{ox} = 1.0 nm, L = 30, 50, 70 and 100 nm, $V_{FB,f}$ = -0.56 V, $V_{FB,b}$ = 0.56 V, mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$

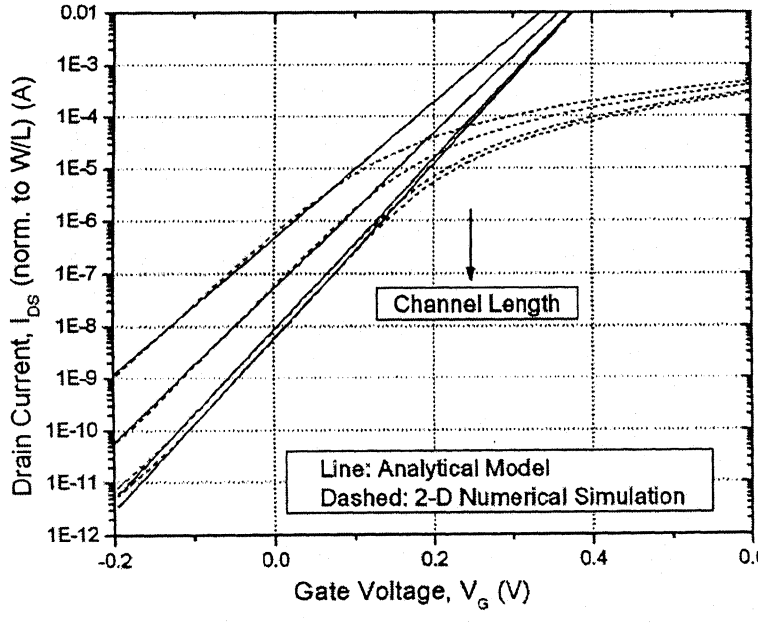

Figure 5.6. Comparison of analytical current model Eq. (5.16) with 2-D atlas simulation for varying lengths. V_{DS}=1.0 V, t_{si} = 20 nm, t_{ox} = 2.0 nm, L = 50, 70, 150 and 300 nm, $V_{FB,f}$ = -0.56 V, $V_{FB,b}$ = 0.56 V, mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$

5.4.2 Sub-threshold Swing Comparison Results

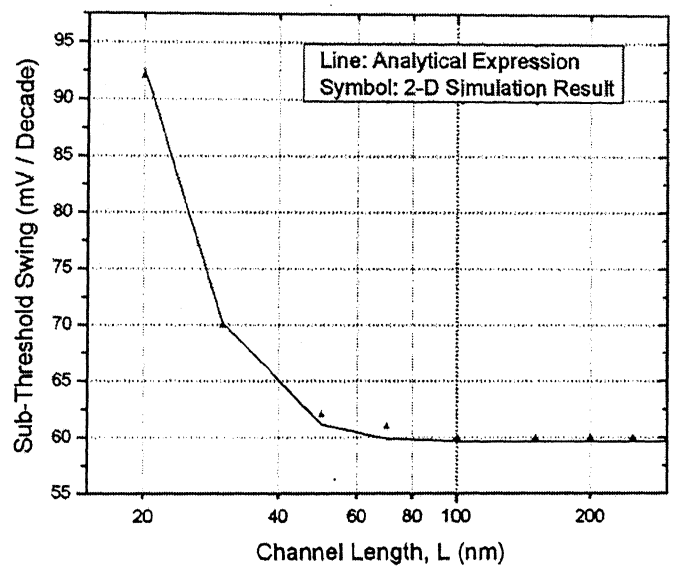

Figure 5.7. Comparison of analytical sub-threshold swing model Eq. (5.20) with 2-D atlas simulation for varying lengths. V_{DS}=1.0 V, t_{si} = 10 nm, t_{ox} = 1.5 nm, L = 20, 30, 50, 70, 100, 150, 200, 250 and 300 nm, $V_{FB,f}$ = -0.56 V, $V_{FB,b}$ = 0.56 V, mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$

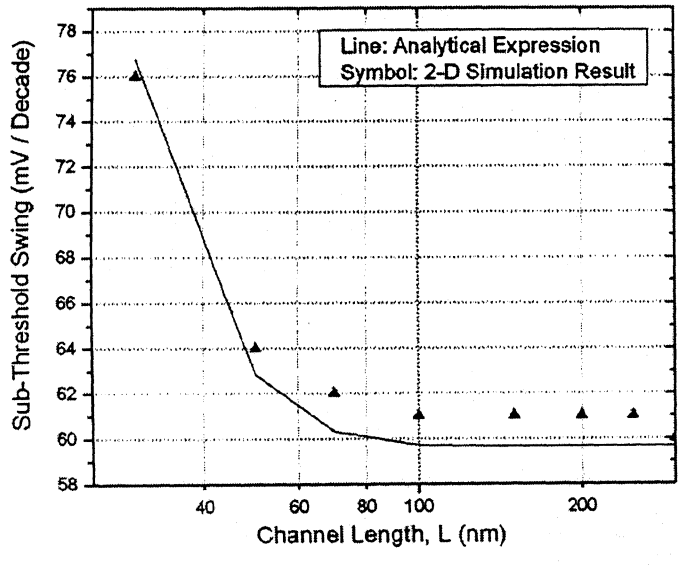

Figure 5.8. Comparison of analytical sub-threshold swing model Eq. (5.20) with 2-D atlas simulation for varying lengths. V_{DS}=1.0 V, t_{si} = 15 nm, t_{ox} = 1.2 nm, L = 30, 50, 70, 100, 150, 200, 250 and 300 nm, $V_{FB,f}$ = -0.56 V, $V_{FB,b}$ = 0.56 V, mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$

Figure 5.7 and figure 5.8 show the comparison of sub-threshold slope values obtained using Eq. (5.20) and those extracted from 2-D Atlas simulation. A good agreement is found between the two showing the validity of Eq. (5.20).

5.4.3 Threshold Voltage Roll-off Comparison

As is done for symmetric DG MOSFET, comparison of threshold voltage roll-off is done for asymmetric DG MOSFET. A good agreement is found between the roll-offs obtained using analytical model results and 2-D simulations results. Along with this the effect of drain voltage on roll-off is also studied. The results of comparisons are shown in figures 5.9-5.12 below. Here also the current is normalized with respect to W/L and current level is taken as 10^{-8} A after normalization for defining the threshold voltage of the device.

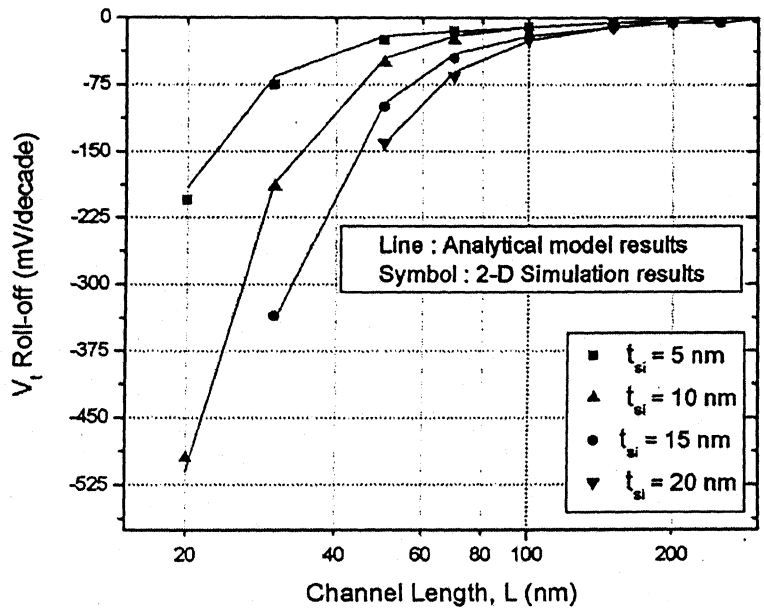

Figure 5.9. Comparison of threshold voltage roll-off obtained from analytical model Eq. (5.16) with 2-D atlas simulation for varying silicon body thickness. V_{DS}=1.0 V, t_{ox} = 2.0 nm, L = 20, 30, 50, 70, 100, 150, 200, 250 and 300 nm, $V_{FB,f}$ = -0.56 V, $V_{FB,b}$ = 0.56 V, mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$

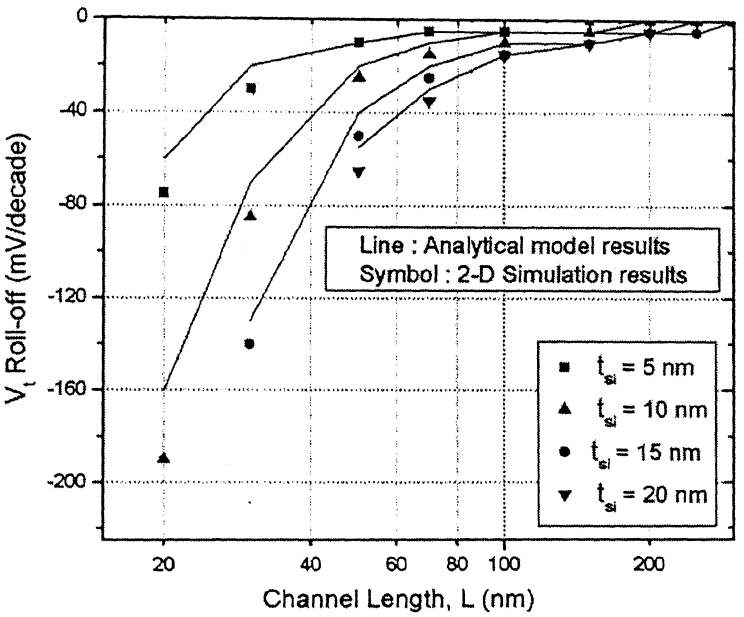

Figure 5.10. Comparison of threshold voltage roll-off obtained from analytical model Eq. (5.16) with 2-D atlas simulation for varying silicon body thickness. V_{DS}=0.01 V, t_{ox} = 1.5 nm, L = 20, 30, 50, 70, 100, 150, 200, 250 and 300 nm, $V_{FB,f}$ = -0.56 V, $V_{FB,b}$ = 0.56 V, mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$

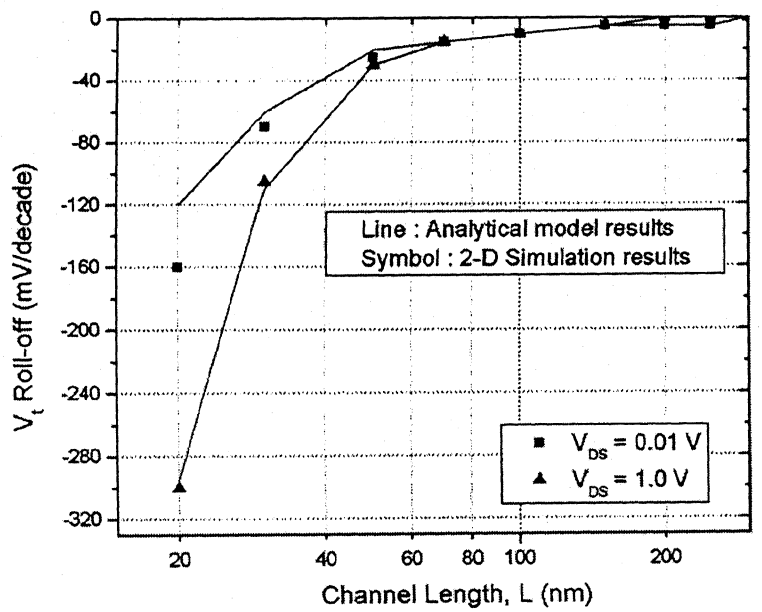

Figure 5.11. Comparison of threshold voltage roll-off obtained from analytical model Eq. (5.16) with 2-D atlas simulation for varying drain bias, showing effect of DIBL. t_{si} = 10 nm, t_{ox} = 1.5 nm, L = 20, 30, 50, 70, 100, 150, 200, 250 and 300 nm, $V_{FB,f}$ = -0.56 V, $V_{FB,b}$ = 0.56 V, mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$

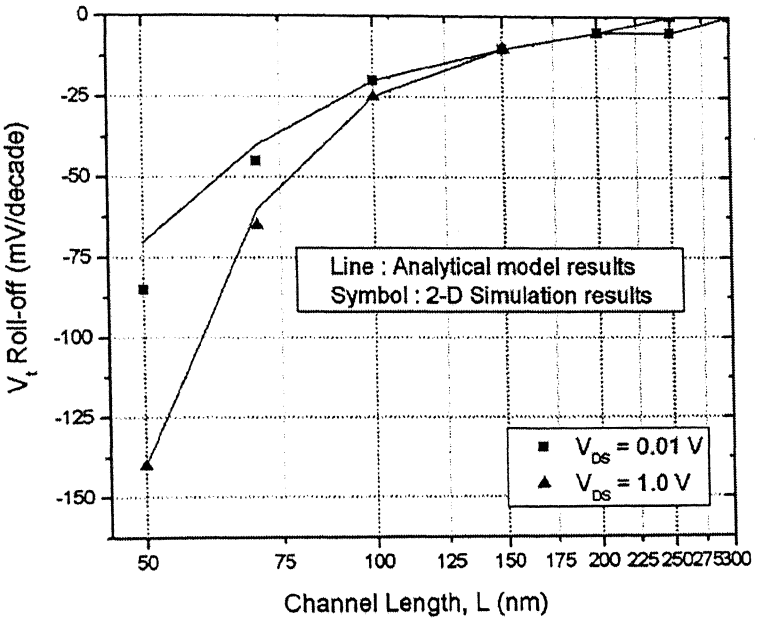

Figure 5.12. Comparison of threshold voltage roll-off obtained from analytical model Eq. (5.16) with 2-D atlas simulation for varying drain bias, showing effect of DIBL. t_{si} = 20 nm, t_{ox} = 2.0 nm, L = 50, 70, 100, 150, 200, 250 and 300 nm, $V_{FB,f}$ = -0.56 V, $V_{FB,b}$ = 0.56 V, mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$

Chapter 6

Symmetric Vs Asymmetric DG MOSFET – A Comparative analysis based on the proposed model

In the previous chapters, models for sub-threshold region for asymmetric and symmetric DG MOSFETs have been presented. There comparison has been done with 2-D device simulator and a good agreement between the two is found showing the validity of models made. But the whole analysis is not complete until a comparison is done between the two modes of operation of these devices and figure out how one mode is better than the other mode. A lot of wok has been done in comparison of these two modes of operation [17],[20]. Most of the work point towards the usefulness of asymmetric devices towards threshold voltage control keeping the similar roll-off values. In this chapter a comparative analysis will be done for both modes based upon the comparison of sub-threshold current, threshold voltage roll-off, the effect of drain induced barrier lowering and sub-threshold slope by comparing two devices of same parameters except change in the gate work function. Finally an attempt is made to come up with a unified model for DG MOSFETs, applicable to both symmetric and asymmetric DG MOSFETs

6.1 Sub-threshold Current Comparison

Figures 6.1 and 6.2 show the comparison of sub-threshold currents of symmetric and asymmetric DG MOSFETs with only difference that for symmetric DG MOSFET, mid-gap gates are considered and for asymmetric DG MOSFET, n+ and p+ gates are considered and all other device parameters are considered same. From the figures it is clear that with same device parameters asymmetric DG MOSFET has lower threshold voltage compared to symmetric DG MOSFET as is also expected as in asymmetric case one gate is n+ so this will have lower threshold voltage and will turn on early. Similar conclusions have been drawn by Yuan Taur [16], where he has commented on the turn-on behaviour of symmetric and asymmetric DG MOSFETs on the basis of inversion charge under the gate in the two cases considered. Thus the results obtained are consistent to what has already been shown by analyzing it in terms of current.

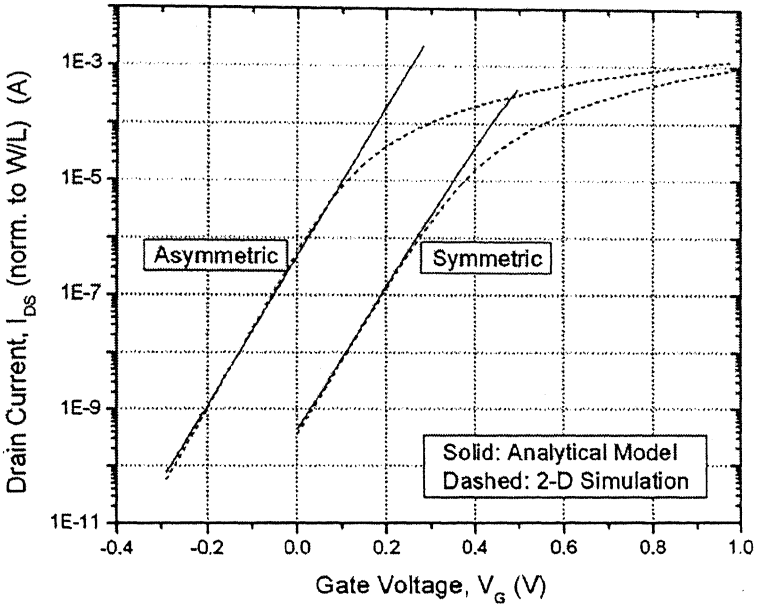

Figure 6.1 : Comparison of symmetric and asymmetric, analytical current model with 2-D atlas simulation. V_{DS}=1.0 V, t_{si} = 20 nm, t_{ox} = 2.0 nm, L = 50 nm, $V_{FB,f} = V_{FB,b}$ = 0 V (symmetric), $V_{FB,f}$ =-0.56 V, $V_{FB,b}$ = 0.56 V (asymmetric), mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$

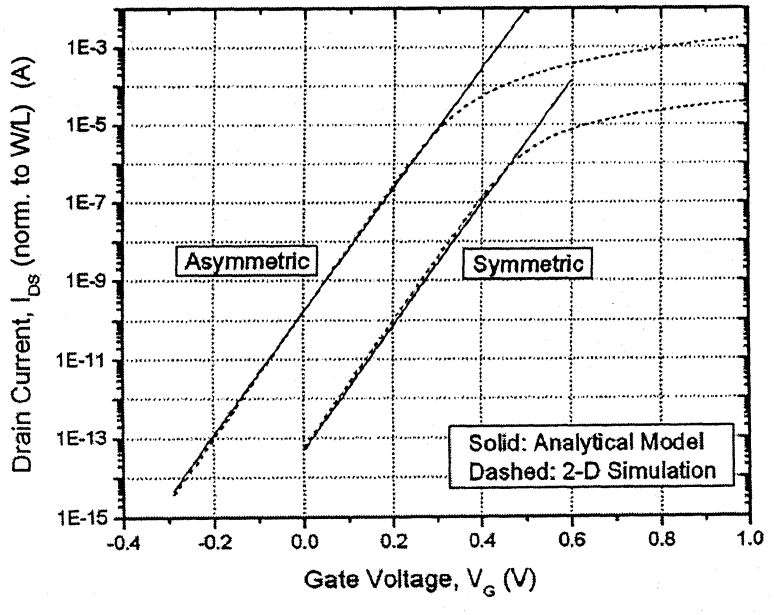

Figure 6.2 : Comparison of symmetric and asymmetric, analytical current model with 2-D atlas simulation. V_{DS}=1.0 V, t_{si} = 5 nm, t_{ox} = 1.0 nm, L = 30 nm, $V_{FB,f} = V_{FB,b}$ = 0 V (symmetric), $V_{FB,f}$ =-0.56 V, $V_{FB,b}$ = 0.56 V (asymmetric), mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$

6.2 Threshold Voltage Roll-off

DG MOSFETs have shown good short-channel immunity due to more gate control. Now as we go on decreasing the silicon body thickness, the gate control is expected to increase on the silicon body and thus resulting in lesser short-channel effects for same lengths. This is what has been observed both for symmetric and asymmetric DG MOSFETs that as one goes on reducing the silicon body thickness, the threshold voltage roll-off reduces for the same channel length. Rephrasing in different way, it can be said that a particular threshold voltage roll-off will occur at larger lengths itself for larger silicon body thickness. This effect has been observed both for symmetric and asymmetric in chapter-3 and chapter-5 respectively. A comparison of roll-off is done between symmetric and asymmetric to see which is more immune to short-channel effects as shown in figures 6.3 and 6.4 below.

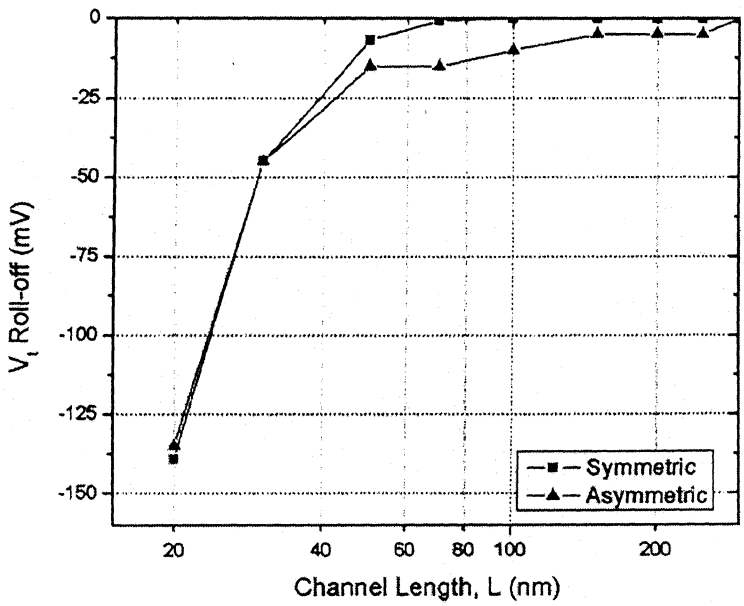

Figure 6.3 : Comparison of symmetric and asymmetric, threshold voltage roll-off. V_{DS}=1.0 V, t_{si} = 5 nm, t_{ox} = 1.5 nm, $V_{FB,f}$ = $V_{FB,b}$ = 0 V (symmetric), $V_{FB,f}$ =-0.56 V, $V_{FB,b}$ = 0.56 V (asymmetric), mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$. Results obtained using the proposed analytical model.

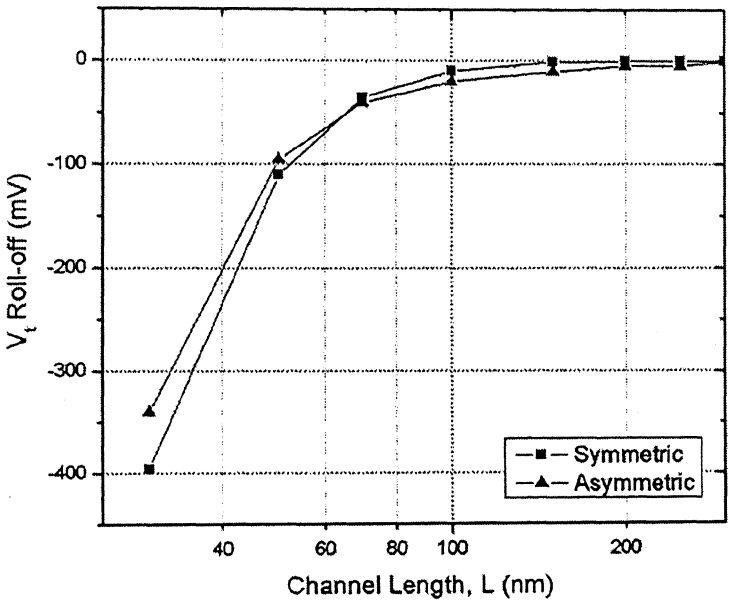

Figure 6.4 : Comparison of symmetric and asymmetric, threshold voltage roll-off. V_{DS}=1.0 V, t_{si} = 15 nm, t_{ox} = 2.0 nm, $V_{FB,f}$ = $V_{FB,b}$ = 0 V (symmetric), $V_{FB,f}$ =-0.56 V, $V_{FB,b}$ = 0.56 V (asymmetric), mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$. Results obtained using the proposed analytical model.

Thus from above two figures one can conclude that both symmetric and asymmetric DG MOSFETs give similar threshold voltage roll-off but asymmetric threshold voltage can be controlled by varying the work functions of the front and back gates. This results in better control over device performance.

6.3 Drain Induced Barrier Lowering

As we increase the drain bias, this effectively results in the decrease in the barrier to the flow of carriers from source to drain and this effect is more prominent for short channel devices. This results in lowering of the threshold voltage of the device. For comparison of the effect of drain bias on the threshold voltage, the parallel shift between the threshold voltage roll-off at V_{DS} = 0.01 V and V_{DS} = 1.0 V is calculated for both symmetric and asymmetric devices and is as shown in figures 6.5 and 6.6.

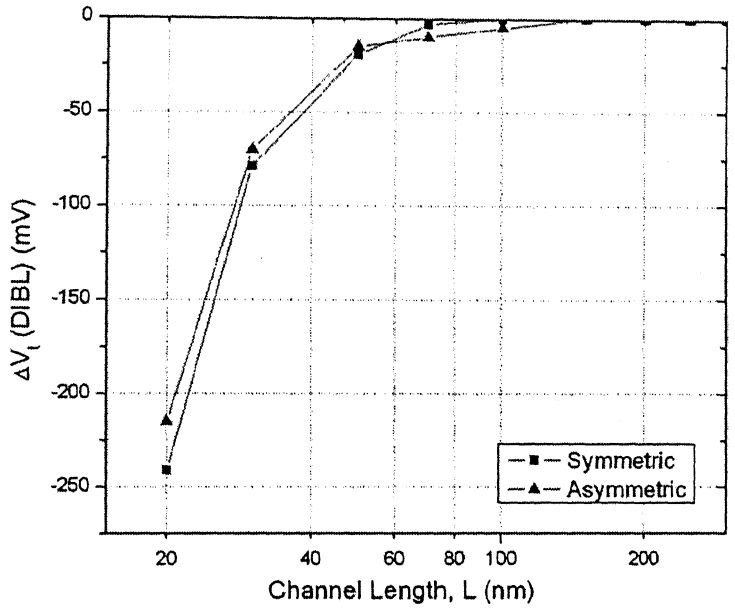

Figure 6.5 : Comparison of symmetric and asymmetric, DIBL effect, VDS=0.01 and 1.0 V, tsi = 10 nm, tox = 1.5 nm, VFB,f = VFB,b = 0 V (symmetric), VFB,f =-0.56 V, VFB,b = 0.56 V (asymmetric), mpbility (μ) = 1400 cm2V-1sec-1. Results obtained using the proposed analytical model.

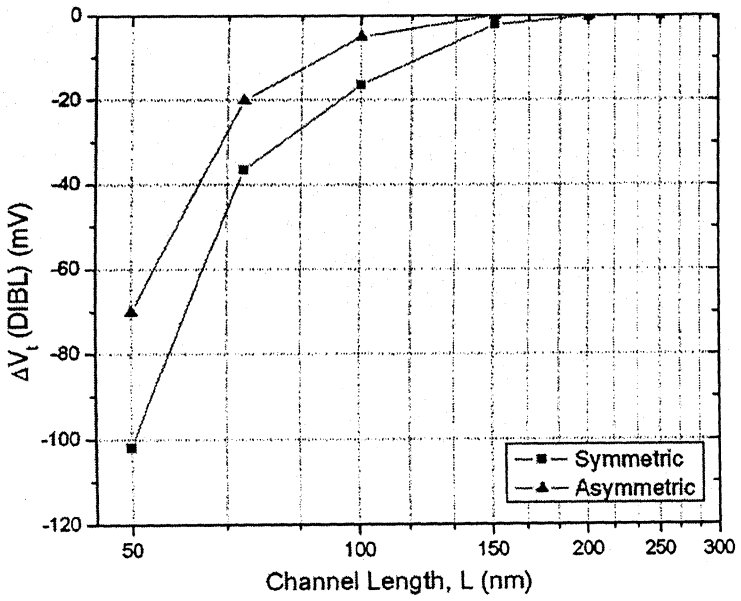

Figure 6.6 : Comparison of symmetric and asymmetric, DIBL effect, V_{DS}=0.01 and 1.0 V, t_{si} = 20 nm, t_{ox} = 2.0 nm, $V_{FB,f}$ = $V_{FB,b}$ = 0 V (symmetric), $V_{FB,f}$ =-0.56 V, $V_{FB,b}$ = 0.56 V (asymmetric), mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$. Results obtained using the proposed analytical model.

Thus from figures 6.5 and 6.6 one can conclude that effect of DIBL is smaller in asymmetric compared to symmetric DG MSOFETs. Similar results have been reported by J.G. Fossum [22], showing the validity of the results obtained.

6.4 Sub-threshold Swing

A comparative analysis of the sub-threshold slope obtained for symmetric and asymmetric DG MOSFETs will be done in this section. Compared slopes were extracted from the 2-D simulation results and also from the sub-threshold swing formulation for both symmetric and asymmetric in chapter-3 and chapter-5 respectively.

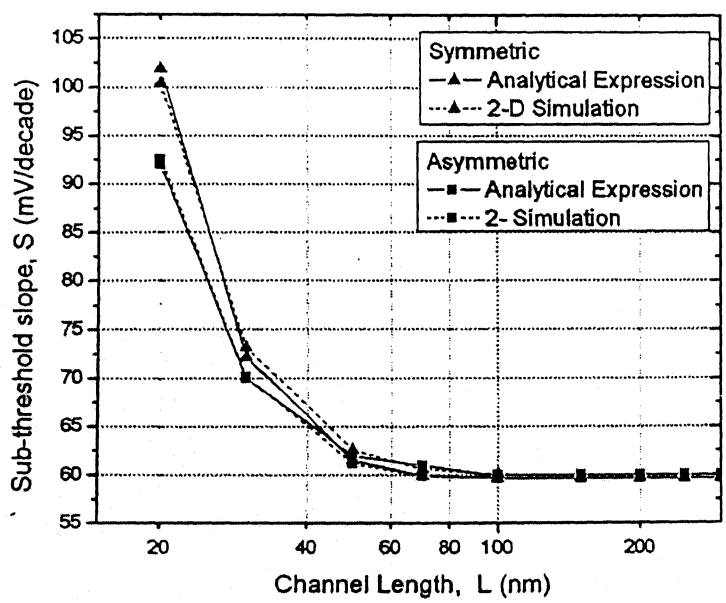

Figure 6.7 : Comparison of symmetric and asymmetric, sub-threshold slope, V_{DS}=1.0 V, t_{si} = 10 nm, t_{ox} = 1.5 nm, $V_{FB,f}$ = $V_{FB,b}$ = 0 V (symmetric), $V_{FB,f}$ =-0.56 V, $V_{FB,b}$ = 0.56 V (asymmetric), mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$. Analytical expression used – Eq. (3.19) (symmetric) and Eq. (5.17) (asymmetric).

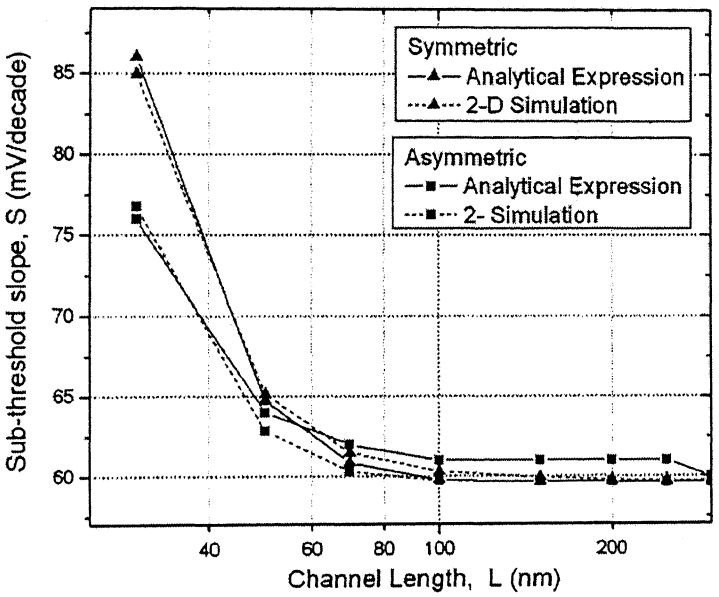

Figure 6.8 : Comparison of symmetric and asymmetric, sub-threshold slope, V_{DS}=1.0 V, t_{si} = 15 nm, t_{ox} = 1.2 nm, $V_{FB,f}$ = $V_{FB,b}$ = 0 V (symmetric), $V_{FB,f}$ =-0.56 V, $V_{FB,b}$ = 0.56 V (asymmetric), mobility (μ) = 1400 $cm^2V^{-1}sec^{-1}$. Analytical expression used – Eq. (3.19) (symmetric) and Eq. (5.17) (asymmetric).

Thus from figure 6.7 & 6.8 one can conclude that both symmetric and asymmetric DG MOSFETs have similar immunity to short channel effects as is indicated by the sub-threshold slope variation with channel length.

All the comparisons done till now show that, in terms of threshold voltage roll-off, DIBL and sub-threshold slope both asymmetric mode and symmetric mode of operation of DG MOSFETs show similar behaviour. But if one looks carefully, then asymmetric DG MOSFET has one main advantage over symmetric and that is the dynamic control over threshold voltage. Because of all these things asymmetric DG MOSFETs have come up as a viable solution for practical applications and are being extensively studied all over the world.

6.5 Unified Sub-threshold Model

The similar behaviour obtained for symmetric and asymmetric devices points that there is a similarity between the two devices and hence an attempt is made to come up with a unified model for DG MOSFETs applicable to both symmetric and asymmetric. Looking carefully at Eq. (3.15) and Eq. (5.16) (repeated below in Eq. (6.1) and Eq. (6.2) for convenience), then both the equations are same except one factor represented by function $f(\varphi_s)$ in Eq. (6.3) below.

For symmetric,

$$I_{DS} = qn_i t_{si}\mu_n \phi_t \frac{W}{L}\exp\left(\frac{\varphi_{s\min}}{\phi_t}\right)\left[1-\exp\left(\frac{-V_{DS}}{\phi_t}\right)\right]$$
$$= qn_i t_{si}\mu_n \phi_t \frac{W}{L}\left[1-\exp\left(\frac{-V_{DS}}{\phi_t}\right)\right] f(\varphi_s) \qquad (6.1)$$

For asymmetric,

$$I_{DS} = qn_i t_{si}\mu_n \phi_t \frac{W}{K.L}\left[1-\exp\left(\frac{-V_{DS}}{\phi_t}\right)\right]$$
$$= qn_i t_{si}\mu_n \phi_t \frac{W}{L}\left[1-\exp\left(\frac{-V_{DS}}{\phi_t}\right)\right] f(\varphi_s) \qquad (6.2)$$

where

$$f(\varphi_s) = \begin{cases} \exp\left(\dfrac{\varphi_{s\min}}{\phi_t}\right) & \textit{for symmetric} \\ \dfrac{1}{K} & \textit{for asymmetric} \end{cases} \qquad (6.3)$$

Here K is given by Eq. (5.14) which is

$$K \approx \left.\frac{\left[\left(\dfrac{\varphi_{s,b}}{\phi_t}\right)-\left(\dfrac{\varphi_{s,f}}{\phi_t}\right)\right]}{\left[\exp\left(\dfrac{\varphi_{s,b}}{\phi_t}\right)-\exp\left(\dfrac{\varphi_{s,f}}{\phi_t}\right)\right]}\right|_{y=y_{\min,b}}$$

Thus one can write a generalized equation for symmetric and asymmetric DG MOSFET

$$I_{DS} = qn_i t_{si}\mu_n \phi_t \frac{W}{L}\left[1-\exp\left(\frac{-V_{DS}}{\phi_t}\right)\right] f(\varphi_s) \qquad (6.4)$$

where $f(\varphi_s)$ is given by Eq. (6.3) in respective cases.

Conclusion and Future Work

Analytical model for sub-threshold region for symmetric and asymmetric DG MOSFETs have been proposed. The models have been verified using 2-D numerical simulator. The unification of models for symmetric and asymmetric DG MOSFETs has been achieved through a surface potential dependent function $f(\varphi_s)$. The strength of the proposed models is that they are physics based, simple and yet are able to predict the device behaviour reasonably accurately. They have potential applications in circuit simulators.

Future Work

DG MOSFETs are in the early stages of development. One of the problems that still remains unresolved is a definition of threshold voltage. This device being used with un-doped silicon body, hence the classical definition of threshold voltage is not applicable to these devices. One has to thus come up with other ways of defining threshold voltage especially for un-doped body devices. There are many definitions available in literature for defining threshold voltage like constant current, maximum slope of trans-conductance etc [23]. But the inherent problem with a definition is either have to define threshold voltage at some arbitrary current level or the introduction of noise in extracting the threshold voltage by using derivative methods. In recent times a new definition for threshold voltage for un-doped body MOSFET has been given which defines the threshold voltage as the point of intersection of the two asymptotes to linear and saturation regions of operation of device [10]. So there is a scope for research in this area.

Appendix A

Derivation for comparison of Surface and Centre Potential

In the derivation of the equations the band structure along with the co-ordinates are as defined in figure A-1 shown below

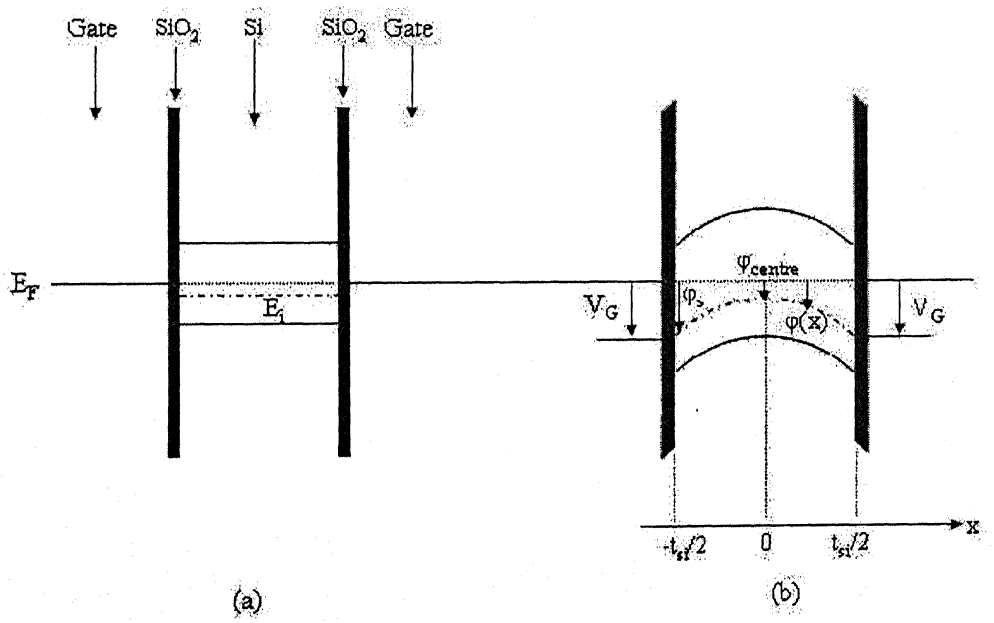

Figure A-1. Schematic band diagram for a symmetric DG MOSFET. (a) At zero gate voltage, assuming near mid-gap gates. (b) Band bending when gate voltage is near threshold voltage.

Since silicon body is not connected to any bias so its Fermi level is referenced with respect to the Fermi level of source Fermi level. Hence mid-gap gates means flat band voltage is zero with respect to that Fermi level of the silicon body.

Now applying Poisson's equation for the silicon body considering only the mobile charge carriers as the body is assumed undoped one gets

$$\frac{d^2\varphi}{dx^2} = \frac{q}{\varepsilon_{si}} n_i \exp\left(\frac{q\varphi}{kT}\right) \tag{A.1}$$

where

q Electronic charge, ε_{si} Permittivity of silicon, n_i Intrinsic carrier density

Eq. (A-1) also assumes that $q\phi/kT >> 1$ so one can neglect the charge due to holes also. Now multiplying both sides of Eq. (A-1) with $2\frac{d\varphi}{dx}$

$$2\frac{d\varphi}{dx}\frac{d^2\varphi}{dx^2}=\frac{2q}{\varepsilon_{si}}n_i\exp\left(\frac{q\varphi}{kT}\right)\frac{d\varphi}{dx}$$

or

$$\frac{d}{dx}\left(\left[\frac{d\varphi}{dx}\right]^2\right)=\frac{2q}{\varepsilon_{si}}n_i\exp\left(\frac{q\varphi}{kT}\right)\frac{d\varphi}{dx} \qquad \text{(A.2)}$$

Integrating Eq. (A-2) from any point x in the silicon body till the centre i.e. at x = 0 as shown in figure A-1 with the following boundary conditions

$$\varphi\big|_{x=x}=\varphi(x) \qquad \text{(i)}$$

$$\varphi\big|_{x=0}=\varphi_{centre} \qquad \text{(ii)}$$

$$\left.\frac{d\varphi}{dx}\right|_{x=0}=0 \qquad \text{(iii)}$$

$$\left(\frac{d\varphi}{dx}\right)^2\Bigg|_{x=0}^{x=x}=\frac{2kT}{\varepsilon_{si}}n_i\exp\left(\frac{q\varphi}{kT}\right)\Bigg|_{\varphi_{centre}}^{\varphi(x)}$$

or

$$\frac{d\varphi(x)}{dx}=\sqrt{\frac{2kTn_i}{\varepsilon_{si}}}\sqrt{\exp\left(\frac{q\varphi(x)}{kT}\right)-\exp\left(\frac{q\varphi_{centre}}{kT}\right)} \qquad \text{(A.3)}$$

Rearranging the terms

$$\frac{d\varphi(x)}{\sqrt{\exp\left(\frac{q\varphi(x)}{kT}\right)-\exp\left(\frac{q\varphi_{centre}}{kT}\right)}}=\sqrt{\frac{2kTn_i}{\varepsilon_{si}}}\,dx \qquad \text{(A.4)}$$

Now integrating Eq. (A-4) again

$$\frac{2kT}{q}\exp\left(\frac{-q\varphi_{centre}}{2kT}\right)\tan^{-1}\left(\frac{\sqrt{\exp\left(\frac{q\varphi(x)}{kT}\right)-\exp\left(\frac{q\varphi_{centre}}{kT}\right)}}{\exp\left(\frac{q\varphi_{centre}}{2kT}\right)}\right)=\sqrt{\frac{2kTn_i}{\varepsilon_{si}}}x$$

or

$$\tan^{-1}\left(\frac{\sqrt{\exp\left(\frac{q\varphi(x)}{kT}\right)-\exp\left(\frac{q\varphi_{centre}}{kT}\right)}}{\exp\left(\frac{q\varphi_{centre}}{2kT}\right)}\right)=\sqrt{\frac{q^2n_i}{2\varepsilon_{si}kT}}\exp\left(\frac{q\varphi_{centre}}{2kT}\right)x$$

or

$$\sqrt{\exp\left(\frac{q\varphi(x)}{kT}\right)-\exp\left(\frac{q\varphi_{centre}}{kT}\right)}=\exp\left(\frac{q\varphi_{centre}}{2kT}\right)\tan\left(\sqrt{\frac{q^2n_i}{2\varepsilon_{si}kT}}\exp\left(\frac{q\varphi_{centre}}{2kT}\right)x\right) \tag{A.5}$$

Still simplifying

$$\exp\left(\frac{q\varphi(x)}{kT}\right)=\exp\left(\frac{q\varphi_{centre}}{kT}\right)\left[1+\tan\left(\sqrt{\frac{q^2n_i}{2\varepsilon_{si}kT}}\exp\left(\frac{q\varphi_{centre}}{2kT}\right)x\right)^2\right]$$

or

$$\exp\left(\frac{q\left(\varphi(x)-\varphi_{centre}\right)}{kT}\right)=\sec\left(\sqrt{\frac{q^2n_i}{2\varepsilon_{si}kT}}\exp\left(\frac{q\varphi_{centre}}{2kT}\right)x\right)^2$$

or

$$\frac{q\left(\varphi(x)-\varphi_{centre}\right)}{2kT}=\ln\left[\sec\left(\sqrt{\frac{q^2n_i}{2\varepsilon_{si}kT}}\exp\left(\frac{q\varphi_{centre}}{2kT}\right)x\right)\right]$$

or

$$\varphi(x)=\varphi_{centre}-\frac{2kT}{q}\ln\left[\cos\left(\sqrt{\frac{q^2n_i}{2\varepsilon_{si}kT}}\exp\left(\frac{q\varphi_{centre}}{2kT}\right)x\right)\right] \tag{A.6}$$

Now surface potential $\varphi_s \equiv \varphi(x)\big|_{x=\pm\frac{t_{si}}{2}}$. Thus from Eq. (A-3) and Eq. (A-6) one gets

$$\frac{d\varphi_s}{dx}=\sqrt{\frac{2kTn_i}{\varepsilon_{si}}}\sqrt{\exp\left(\frac{q\varphi_s}{kT}\right)-\exp\left(\frac{q\varphi_{centre}}{kT}\right)} \tag{A.7}$$

and

$$\varphi_s=\varphi_{centre}-\frac{2kT}{q}\ln\left[\cos\left(\sqrt{\frac{q^2n_i}{2\varepsilon_{si}kT}}\exp\left(\frac{q\varphi_{centre}}{2kT}\right)\frac{t_{si}}{2}\right)\right] \tag{A.8}$$

Now surface potential is related to the gate voltage V_G and oxide thickness t_{ox} at Si-SiO_2 interface by Gauss's law given as

$$\varepsilon_{ox}\frac{V_G - V_{FB} - \varphi_s}{t_{ox}} = \pm\varepsilon_{si}\left.\frac{d\varphi(x)}{dx}\right|_{x=\pm\frac{t_{si}}{2}}$$

or

$$V_G - V_{FB} = \varphi_s \pm \frac{\varepsilon_{si}t_{ox}}{\varepsilon_{ox}}\left.\frac{d\varphi(x)}{dx}\right|_{x=\pm\frac{t_{si}}{2}} = \varphi_s \pm \frac{\varepsilon_{si}}{C_{ox}}\left.\frac{d\varphi(x)}{dx}\right|_{x=\pm\frac{t_{si}}{2}} \tag{A.9}$$

Now substituting, $\theta = \sqrt{\frac{q^2 n_i}{2\varepsilon_{si}kT}}\exp\left(\frac{q\varphi_{centre}}{2kT}\right)\frac{t_{si}}{2}$ and using Eq. (A-3) and Eq. (A-6)

$$\frac{d\varphi_s}{dx} = \sqrt{\frac{2kTn_i}{\varepsilon_{si}}}\exp\left(\frac{q\varphi_{centre}}{2kT}\right)\tan(\theta) \tag{A.10}$$

Also Eq. (A-8) becomes

$$\varphi_s = \varphi_{centre} - \frac{2kT}{q}\ln\left[\cos(\theta)\right] \tag{A.11}$$

Thus from Eq. (A.9), Eq. (A.10) and Eq. (A.11) one gets

$$V_G - V_{FB} = \varphi_{centre} - \frac{2kT}{q}\ln\left[\cos(\theta)\right] - \frac{\sqrt{2\varepsilon_{si}kTn_i}}{C_{ox}}\exp\left(\frac{q\varphi_{centre}}{2kT}\right)\tan(\theta) \tag{A.12}$$

Eq. (A.12) and Eq. (A.11) now form Eq. (2.3) and Eq. (2.4) respectively in chapter 2. Eq. (A.12) can be solved using any of the commonly known numerical methods. For the present case Newton-Raphson method has been used for solving it.

Appendix B

Derivation of Surface Potential expression along the channel for Symmetric DG MOSFETs

From Eq. (2.8) one has

$$\frac{d^2\varphi_s(y)}{dy^2} = \frac{1}{\lambda^2}\left[\varphi_s(y) - (V_G - V_{FB})\right] \tag{B.1}$$

Also the following boundary conditions are there from section 2.3

$$\varphi_s(0) = \varphi(x,0) = \phi_{bi} \tag{I}$$

$$\varphi_s(L) = \varphi(x,L) = \phi_{bi} + V_{DS} \tag{II}$$

Let $\varphi_s(y) - (V_G - V_{FB}) = Z(y)$, thus

$$\frac{d^2\varphi_s(y)}{dy^2} = \frac{d^2Z(y)}{dy^2}$$

Putting these values into Eq. (B.1)

$$\frac{d^2Z(y)}{dy^2} = \frac{Z(y)}{\lambda^2} \tag{B.2}$$

Now Eq. (B.2) is a standard wave equation with the following form of solution

$$Z(y) = A\sinh\left(\frac{y}{\lambda}\right) + B\cosh\left(\frac{y}{\lambda}\right) \tag{B.3}$$

Putting back value of $Z(y)$

$$\varphi_s(y) = V_G - V_{FB} + A\sinh\left(\frac{y}{\lambda}\right) + B\cosh\left(\frac{y}{\lambda}\right) \tag{B.4}$$

Now using boundary conditions (I) and (II) the following equations are obtained

$$\varphi_s(0) = \phi_{bi} = V_G - V_{FB} + B \tag{B.5}$$

$$\varphi_s(L) = \phi_{bi} + V_{DS} = V_G - V_{FB} + A\sinh\left(\frac{L}{\lambda}\right) + B\cosh\left(\frac{L}{\lambda}\right) \tag{B.6}$$

Thus

$$B = \varphi_s(0) - V_{Geff} \qquad \text{and} \qquad A = \frac{\left[\varphi_s(L) - V_{Geff}\right]}{\sinh\left(\frac{L}{\lambda}\right)} - \frac{\left[\varphi_s(0) - V_{Geff}\right]}{\sinh\left(\frac{L}{\lambda}\right)}\cosh\left(\frac{L}{\lambda}\right)$$

where $V_{Geff} = V_G - V_{FB}$

Putting back values of A and B in Eq. (B.4) one gets

$$\varphi_s(y) = V_{Geff} + \frac{[\varphi_s(L) - V_{Geff}]\sinh\left(\frac{y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)} - \frac{[\varphi_s(0) - V_{Geff}]\cosh\left(\frac{L}{\lambda}\right)\sinh\left(\frac{y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}$$

$$+ \frac{[\varphi_s(0) - V_{Geff}]\cosh\left(\frac{y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}$$

or

$$\varphi_s(y) = V_{Geff} + \frac{[\varphi_s(L) - V_{Geff}]\sinh\left(\frac{y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}$$

$$+ \frac{[\varphi_s(0) - V_{Geff}]\left[\cosh\left(\frac{y}{\lambda}\right)\sinh\left(\frac{L}{\lambda}\right) - \cosh\left(\frac{L}{\lambda}\right)\sinh\left(\frac{y}{\lambda}\right)\right]}{\sinh\left(\frac{L}{\lambda}\right)}$$

or

$$\varphi_s(y) = V_{Geff} + \frac{[\varphi_s(L) - V_{Geff}]\sinh\left(\frac{y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)} + \frac{[\varphi_s(0) - V_{Geff}]\sinh\left(\frac{L-y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)} \qquad \text{(B.7)}$$

Thus Eq. (B.7) forms Eq. (2.9) in chapter 2.

Appendix C

Minimum Surface Potential along the channel derivation for Symmetric DG MOSFETs

Minimum Surface potential point:

From Eq. (2.9) one has

$$\varphi_s(y) = V_{Geff} + \left(\varphi_s(0) - V_{Geff}\right)\left(\frac{\sinh\left(\frac{L-y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}\right) + \left(\varphi_s(L) - V_{Geff}\right)\left(\frac{\sinh\left(\frac{y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}\right) \qquad \text{(C.1)}$$

Now differentiating and equating it to zero will give point along channel (y_{min}) where surface potential will be minimum

$$\frac{d\varphi_s(y)}{dy} = -\left(\frac{\varphi_s(0) - V_{Geff}}{\lambda}\right)\left(\frac{\cosh\left(\frac{L-y_{\min}}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}\right) + \left(\frac{\varphi_s(L) - V_{Geff}}{\lambda}\right)\left(\frac{\cosh\left(\frac{y_{\min}}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}\right) = 0$$

or

$$\frac{\cosh\left(\frac{y_{\min}}{\lambda}\right)}{\cosh\left(\frac{L-y_{\min}}{\lambda}\right)} = \left(\frac{\varphi_s(0) - V_{Geff}}{\varphi_s(L) - V_{Geff}}\right)$$

or

$$\frac{\exp\left(\frac{y_{\min}}{\lambda}\right) + \exp\left(\frac{-y_{\min}}{\lambda}\right)}{\exp\left(\frac{L-y_{\min}}{\lambda}\right) + \exp\left(\frac{y_{\min}-L}{\lambda}\right)} = \left(\frac{\varphi_s(0) - V_{Geff}}{\varphi_s(L) - V_{Geff}}\right)$$

or

$$\left[\exp\left(\frac{y_{\min}}{\lambda}\right) + \exp\left(\frac{-y_{\min}}{\lambda}\right)\right]\left(\varphi_s(L) - V_{Geff}\right) = \left[\exp\left(\frac{L-y_{\min}}{\lambda}\right) + \exp\left(\frac{y_{\min}-L}{\lambda}\right)\right]\left(\varphi_s(0) - V_{Geff}\right)$$

or

$$\left[\left(\varphi_s(L)-V_{Geff}\right)-\left(\varphi_s(0)-V_{Geff}\right)\exp\left(\frac{-L}{\lambda}\right)\right]\exp\left(\frac{y}{\lambda}\right)$$

$$=\left[\left(\varphi_s(0)-V_{Geff}\right)\exp\left(\frac{L}{\lambda}\right)-\left(\varphi_s(L)-V_{Geff}\right)\right]\exp\left(\frac{-y}{\lambda}\right)$$

or

$$\exp\left(\frac{2y_{\min}}{\lambda}\right)=\frac{\left[\left(\varphi_s(0)-V_{Geff}\right)\exp\left(\frac{L}{\lambda}\right)-\left(\varphi_s(L)-V_{Geff}\right)\right]}{\left[\left(\varphi_s(L)-V_{Geff}\right)-\left(\varphi_s(0)-V_{Geff}\right)\exp\left(\frac{-L}{\lambda}\right)\right]}$$

Finally one gets

$$y_{\min}=\frac{\lambda}{2}\ln\left[\frac{\left(\varphi_s(0)-V_{Geff}\right)\exp\left(\frac{L}{\lambda}\right)-\left(\varphi_s(L)-V_{Geff}\right)}{\left(\varphi_s(L)-V_{Geff}\right)-\left(\varphi_s(0)-V_{Geff}\right)\exp\left(\frac{-L}{\lambda}\right)}\right] \tag{C.2}$$

Thus Eq. (C.2) is giving Eq. (3.13) in chapter 3.

Minimum surface potential:

Minimum surface potential along the channel is obtained by evaluating Eq. (C.1) at y_{min}. Now

$$\exp\left(\frac{y_{\min}}{\lambda}\right)=\frac{\left[\left(\varphi_s(0)-V_{Geff}\right)\exp\left(\frac{L}{\lambda}\right)-\left(\varphi_s(L)-V_{Geff}\right)\right]^{1/2}}{\left[\left(\varphi_s(L)-V_{Geff}\right)-\left(\varphi_s(0)-V_{Geff}\right)\exp\left(\frac{-L}{\lambda}\right)\right]^{1/2}} \tag{C.3}$$

$$\exp\left(\frac{-y_{\min}}{\lambda}\right)=\frac{\left[\left(\varphi_s(L)-V_{Geff}\right)-\left(\varphi_s(0)-V_{Geff}\right)\exp\left(\frac{-L}{\lambda}\right)\right]^{1/2}}{\left[\left(\varphi_s(0)-V_{Geff}\right)\exp\left(\frac{L}{\lambda}\right)-\left(\varphi_s(L)-V_{Geff}\right)\right]^{1/2}} \tag{C.4}$$

$$\exp\left(\frac{L-y_{\min}}{\lambda}\right)=\frac{\exp\left(\frac{L}{\lambda}\right)\left[\left(\varphi_s(L)-V_{Geff}\right)-\left(\varphi_s(0)-V_{Geff}\right)\exp\left(\frac{-L}{\lambda}\right)\right]^{1/2}}{\left[\left(\varphi_s(0)-V_{Geff}\right)\exp\left(\frac{L}{\lambda}\right)-\left(\varphi_s(L)-V_{Geff}\right)\right]^{1/2}} \tag{C.5}$$

$$\exp\left(\frac{y_{\min}-L}{\lambda}\right)=\frac{\exp\left(\frac{-L}{\lambda}\right)\left[\left(\varphi_s(0)-V_{Geff}\right)\exp\left(\frac{L}{\lambda}\right)-\left(\varphi_s(L)-V_{Geff}\right)\right]^{1/2}}{\left[\left(\varphi_s(L)-V_{Geff}\right)-\left(\varphi_s(0)-V_{Geff}\right)\exp\left(\frac{-L}{\lambda}\right)\right]^{1/2}} \qquad \text{(C.6)}$$

From Eq. (C.3) and Eq. (C.4) one can get

$$\sinh\left(\frac{y_{\min}}{\lambda}\right)=\frac{\exp\left(\frac{y_{\min}}{\lambda}\right)-\exp\left(\frac{-y_{\min}}{\lambda}\right)}{2}$$

$$=\frac{1}{2}\frac{\left[\left(\varphi_s(0)-V_{Geff}\right)\exp\left(\frac{L}{\lambda}\right)-\left(\varphi_s(L)-V_{Geff}\right)\right]^{1/2}}{\left[\left(\varphi_s(L)-V_{Geff}\right)-\left(\varphi_s(0)-V_{Geff}\right)\exp\left(\frac{-L}{\lambda}\right)\right]^{1/2}}$$

$$-\frac{1}{2}\frac{\left[\left(\varphi_s(L)-V_{Geff}\right)-\left(\varphi_s(0)-V_{Geff}\right)\exp\left(\frac{-L}{\lambda}\right)\right]^{1/2}}{\left[\left(\varphi_s(0)-V_{Geff}\right)\exp\left(\frac{L}{\lambda}\right)-\left(\varphi_s(L)-V_{Geff}\right)\right]^{1/2}}$$

$$=\frac{1}{2}\frac{\left(\varphi_s(0)-V_{Geff}\right)\exp\left(\frac{L}{\lambda}\right)-\left(\varphi_s(L)-V_{Geff}\right)-\left(\varphi_s(L)-V_{Geff}\right)+\left(\varphi_s(0)-V_{Geff}\right)\exp\left(\frac{-L}{\lambda}\right)}{\left\{\left[\left(\varphi_s(L)-V_{Geff}\right)-\left(\varphi_s(0)-V_{Geff}\right)\exp\left(\frac{-L}{\lambda}\right)\right]\left[\left(\varphi_s(0)-V_{Geff}\right)\exp\left(\frac{L}{\lambda}\right)-\left(\varphi_s(L)-V_{Geff}\right)\right]\right\}^{1/2}}$$

$$=\frac{\left(\varphi_s(0)-V_{Geff}\right)\left[\frac{\exp\left(\frac{L}{\lambda}\right)+\exp\left(\frac{-L}{\lambda}\right)}{2}\right]-\left(\varphi_s(L)-V_{Geff}\right)}{F}$$

$$=\frac{\left(\varphi_s(0)-V_{Geff}\right)\cosh\left(\frac{L}{\lambda}\right)-\left(\varphi_s(L)-V_{Geff}\right)}{F} \qquad \text{(C.7)}$$

where

$$F=\left\{\left[\left(\varphi_s(L)-V_{Geff}\right)-\left(\varphi_s(0)-V_{Geff}\right)\exp\left(\frac{-L}{\lambda}\right)\right]\left[\left(\varphi_s(0)-V_{Geff}\right)\exp\left(\frac{L}{\lambda}\right)-\left(\varphi_s(L)-V_{Geff}\right)\right]\right\}^{1/2}$$

Similarly using Eq. (C.5) and Eq. (C.6) one can show

$$\sinh\left(\frac{L-y_{\min}}{\lambda}\right)=\frac{(\varphi_s(0)-V_{Geff})\cosh\left(\frac{L}{\lambda}\right)-(\varphi_s(L)-V_{Geff})}{F} \qquad \text{(C.8)}$$

Further simplification of F leads to,

$$F=\left\{(\varphi_s(L)-V_{Geff})(\varphi_s(0)-V_{Geff})\left[\exp\left(\frac{L}{\lambda}\right)+\exp\left(\frac{-L}{\lambda}\right)\right]-(\varphi_s(0)-V_{Geff})^2-(\varphi_s(L)-V_{Geff})^2\right\}^{1/2}$$

$$=\left[2\cosh\left(\frac{L}{\lambda}\right)(\varphi_s(L)-V_{Geff})(\varphi_s(0)-V_{Geff})-(\varphi_s(0)-V_{Geff})^2-(\varphi_s(L)-V_{Geff})^2\right]^{1/2}$$

$$=\left[\left(2\cosh\left(\frac{L}{\lambda}\right)-2\right)(\varphi_s(L)-V_{Geff})(\varphi_s(0)-V_{Geff})-[(\varphi_s(L)-V_{Geff})-(\varphi_s(0)-V_{Geff})]^2\right]^{1/2}$$

$$=\left[2C_2(\varphi_s(L)-V_{Geff})(\varphi_s(0)-V_{Geff})-[\varphi_s(L)-\varphi_s(0)]^2\right]^{1/2}$$

$$=\left[2C_2(\varphi_s(L)-V_{Geff})(\varphi_s(0)-V_{Geff})-V_{DS}^2\right]^{1/2}$$

where

$$C_2=\cosh\left(\frac{L}{\lambda}\right)-1 \quad \text{And} \quad \varphi_s(L)-\varphi_s(0)=V_{DS}$$

Thus putting y_{min} in Eq. (C.1) one gets

$$\varphi_{s\,\min}=V_{Geff}+(\varphi_s(0)-V_{Geff})\left(\frac{\sinh\left(\frac{L-y_{\min}}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}\right)+(\varphi_s(L)-V_{Geff})\left(\frac{\sinh\left(\frac{y_{\min}}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}\right)$$

Using Eq. (C.7) and Eq. (C.8) one can solve for $\varphi_{s\,\min}$ to get

$$\varphi_{s\,\min}=V_{Geff}+\frac{(\varphi_s(0)-V_{Geff})\left[(\varphi_s(L)-V_{Geff})\cosh\left(\frac{L}{\lambda}\right)-(\varphi_s(0)-V_{Geff})\right]}{F\sinh\left(\frac{L}{\lambda}\right)}$$

$$+\frac{(\varphi_s(L)-V_{Geff})\left[(\varphi_s(0)-V_{Geff})\cosh\left(\frac{L}{\lambda}\right)-(\varphi_s(L)-V_{Geff})\right]}{F\sinh\left(\frac{L}{\lambda}\right)}$$

$$= V_{Geff} + \frac{(\varphi_s(0) - V_{Geff})(\varphi_s(L) - V_{Geff})\cosh\left(\frac{L}{\lambda}\right) - (\varphi_s(0) - V_{Geff})^2}{F\sinh\left(\frac{L}{\lambda}\right)}$$

$$+ \frac{(\varphi_s(0) - V_{Geff})(\varphi_s(L) - V_{Geff})\cosh\left(\frac{L}{\lambda}\right) - (\varphi_s(L) - V_{Geff})^2}{F\sinh\left(\frac{L}{\lambda}\right)}$$

$$= V_{Geff} + \frac{\left[2\cosh\left(\frac{L}{\lambda}\right)(\varphi_s(L) - V_{Geff})(\varphi_s(0) - V_{Geff}) - (\varphi_s(0) - V_{Geff})^2 - (\varphi_s(L) - V_{Geff})^2\right]}{F\sinh\left(\frac{L}{\lambda}\right)}$$

$$= V_{Geff} + \frac{F^2}{F\sinh\left(\frac{L}{\lambda}\right)} = V_{Geff} + \frac{F}{\sinh\left(\frac{L}{\lambda}\right)}$$

Finally one obtains,

$$\varphi_{s\,\min} = V_{Geff} + \frac{1}{C_1}\left[2C_2(\varphi_s(L) - V_{Geff})(\varphi_s(0) - V_{Geff}) - V_{DS}^2\right]^{1/2} \qquad \text{(C.9)}$$

where

$$C_1 = \sinh\left(\frac{L}{\lambda}\right) \quad \text{and} \quad C_2 = \cosh\left(\frac{L}{\lambda}\right) - 1$$

Thus Eq. (3.14) in chapter 3 represents Eq. (C.9).

Appendix D

Integration of carrier density perpendicular to channel

Starting with Eq. (5.5)

$$n(x,y) = n_i \exp\left(\frac{\varphi(x,y) - V_{channel}(y)}{\phi_t}\right) \tag{D.1}$$

Also from Eq. (4.6) one gets

$$\varphi(x,y) = \frac{(\varphi_{s,b} - \varphi_{s,f})}{t_{si}} x + \frac{(\varphi_{s,b} + \varphi_{s,f})}{2} \tag{D.2}$$

Substituting Eq. (D.2) in Eq. (D.1),

$$n(x,y) = n_i \exp\left(\frac{-V_{channel}(y)}{\phi_t}\right) \exp\left(\frac{\varphi_{s,b} + \varphi_{s,f}}{2\phi_t}\right) \exp\left(\frac{\varphi_{s,b} - \varphi_{s,f}}{\phi_t} \cdot \frac{x}{t_{si}}\right)$$

or

$$n(x,y) = N \exp\left(\frac{\varphi_{s,b} - \varphi_{s,f}}{\phi_t} \cdot \frac{x}{t_{si}}\right) \tag{D.3}$$

where $N = n_i \exp\left(\frac{-V_{channel}(y)}{\phi_t}\right) \exp\left(\frac{\varphi_{s,b} + \varphi_{s,f}}{2\phi_t}\right)$

Now integrating Eq. (D.3) from top surface to bottom surface of silicon body,

$$n(y) = \int_{-t_{si}/2}^{t_{si}/2} n(x,y)\,dx = \int_{-t_{si}/2}^{t_{si}/2} N \exp\left(\frac{\varphi_{s,b} - \varphi_{s,f}}{\phi_t} \cdot \frac{x}{t_{si}}\right) dx$$

$$= N t_{si} \left| \frac{\exp\left(\frac{\varphi_{s,b} - \varphi_{s,f}}{\phi_t} \cdot \frac{x}{t_{si}}\right)}{\frac{\varphi_{s,b} - \varphi_{s,f}}{\phi_t}} \right|_{-t_{si}/2}^{t_{si}/2}$$

$$= N t_{si} \left[\frac{\exp\left(\frac{\varphi_{s,b} - \varphi_{s,f}}{2\phi_t}\right) - \exp\left(\frac{\varphi_{s,f} - \varphi_{s,b}}{2\phi_t}\right)}{\frac{\varphi_{s,b} - \varphi_{s,f}}{\phi_t}} \right] \tag{D.4}$$

D.4) one gets

$$n(y) = n_i\, t_{si}\, \exp\left(\frac{-V_{channel}(y)}{\phi_t}\right)\left[\frac{\exp\left(\frac{\varphi_{s,b}}{\phi_t}\right) - \exp\left(\frac{\varphi_{s,f}}{\phi_t}\right)}{\frac{\varphi_{s,b} - \varphi_{s,f}}{\phi_t}}\right]. \qquad \text{(D.5)}$$

Thus Eq. (D.5) is used in chapter 5 as Eq. (5.8).

Appendix E

Mathematical Analysis for asymmetric DG MOSFET sub-threshold slope

From Eq. (5.18) one has

$$\frac{d\left(\ln I_{DS}\right)}{dV_G} = -\frac{d\ln K}{dV_G} = -\frac{1}{K}\frac{dK}{dV_G} \tag{E.1}$$

Also from Eq. (5.14) the value of K can be written as

$$K = \left.\frac{\left[\left(\frac{\varphi_{s,b}}{\phi_t}\right) - \left(\frac{\varphi_{s,f}}{\phi_t}\right)\right]}{\left[\exp\left(\frac{\varphi_{s,b}}{\phi_t}\right) - \exp\left(\frac{\varphi_{s,f}}{\phi_t}\right)\right]}\right|_{y=y_{\min,b}} \tag{E.2}$$

Differentiating Eq. (E.2) with respect to V_G

$$\frac{dK}{dV_G} = \left.\frac{\frac{1}{\phi_t}\left[\left(\frac{d\varphi_{s,b}}{dV_G}\right) - \left(\frac{d\varphi_{s,f}}{dV_G}\right)\right]}{\left[\exp\left(\frac{\varphi_{s,b}}{\phi_t}\right) - \exp\left(\frac{\varphi_{s,f}}{\phi_t}\right)\right]}\right|_{y=y_{\min,b}}$$

$$\left. - \frac{\frac{1}{\phi_t}\left[\exp\left(\frac{\varphi_{s,b}}{\phi_t}\right)\left(\frac{d\varphi_{s,b}}{dV_G}\right) - \exp\left(\frac{\varphi_{s,f}}{\phi_t}\right)\left(\frac{d\varphi_{s,f}}{dV_G}\right)\right]\left[\left(\frac{\varphi_{s,b}}{\phi_t}\right) - \left(\frac{\varphi_{s,f}}{\phi_t}\right)\right]}{\left[\exp\left(\frac{\varphi_{s,b}}{\phi_t}\right) - \exp\left(\frac{\varphi_{s,f}}{\phi_t}\right)\right]^2}\right|_{y=y_{\min,b}} \tag{E.3}$$

Now from Eq. (4.17) and Eq. (4.18) one gets

$$\varphi_{s,f}(y) = V_{Geff,f} + \left(\varphi_{s,f}(0) - V_{Geff,f}\right)\left(\frac{\sinh\left(\frac{L-y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}\right) + \left(\varphi_{s,f}(L) - V_{Geff,f}\right)\left(\frac{\sinh\left(\frac{y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}\right) \tag{E.4}$$

$$\varphi_{s,b}(y) = V_{Geff,b} + \left(\varphi_{s,b}(0) - V_{Geff,b}\right)\left(\frac{\sinh\left(\frac{L-y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}\right) + \left(\varphi_{s,b}(L) - V_{Geff,b}\right)\left(\frac{\sinh\left(\frac{y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}\right) \tag{E.5}$$

Differentiating Eq. (E.4) with respect to V_G, one obtains

$$\frac{d\varphi_{s,f}(y)}{dV_G} = 1 - \left(\frac{\sinh\left(\frac{L-y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)} \right) - \left(\frac{\sinh\left(\frac{y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)} \right) \tag{E.6}$$

Similarly by differentiating Eq. (E.5), one gets

$$\frac{d\varphi_{s,b}(y)}{dV_G} = 1 - \left(\frac{\sinh\left(\frac{L-y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)} \right) - \left(\frac{\sinh\left(\frac{y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)} \right) \tag{E.7}$$

From Eq. (E.6) and Eq. (E.7) one can infer

$$\frac{d\varphi_{s,b}(y)}{dV_G} = \frac{d\varphi_{s,f}(y)}{dV_G} \tag{E.8}$$

Using Eq. (E.8) in Eq. (E.3), one gets

$$\frac{dK}{dV_G} = -\left. \frac{\frac{1}{\phi_t}\left(\frac{d\varphi_{s,b}}{dV_G}\right)\left[\left(\frac{\varphi_{s,b}}{\phi_t}\right) - \left(\frac{\varphi_{s,f}}{\phi_t}\right)\right]}{\left[\exp\left(\frac{\varphi_{s,b}}{\phi_t}\right) - \exp\left(\frac{\varphi_{s,f}}{\phi_t}\right)\right]} \right|_{y=y_{min,b}}$$

or

$$\frac{dK}{dV_G} = -\frac{K}{\phi_t}\left(\frac{d\varphi_{s,b}}{dV_G}\right)\Bigg|_{y=y_{min,b}}$$

or

$$-\frac{1}{K}\frac{dK}{dV_G} = \frac{1}{\phi_t}\left(\frac{d\varphi_{s,b}}{dV_G}\right)\Bigg|_{y=y_{min,b}} \tag{E.9}$$

Putting Eq. (E.9) in Eq. (E.1)

$$\frac{d\left(\ln I_{DS}\right)}{dV_G} = -\frac{d\ln K}{dV_G} = -\frac{1}{K}\frac{dK}{dV_G} = \frac{1}{\phi_t}\frac{d\varphi_{s,b}}{dV_G}\Bigg|_{y=y_{min,b}} \tag{E.10}$$

With the help of Eq. (E.8) in Eq. (E.10) one finally gets

$$\frac{d\ln I_{DS}}{dV_G} = \frac{1}{\phi_t}\left[1 - \left(\frac{\sinh\left(\frac{L-y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}\right) - \left(\frac{\sinh\left(\frac{y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}\right)\right] \tag{E.11}$$

Thus Eq. (E.11) is used as Eq. (5.19) in chapter 5.

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